



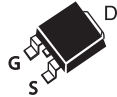
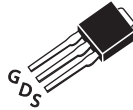
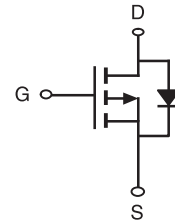
## P-Channel Logic Level Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
-40V	-32A	16 @ V <sub>GS</sub> =-10V
		30 @ V <sub>GS</sub> =-4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.

STU SERIES  
TO-252AA(D-PAK)STD SERIES  
TO-251(I-PAK)

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	-40	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a e</sup>	T <sub>C</sub> =25°C	-32
		T <sub>C</sub> =70°C	-25.6
I <sub>DM</sub>	-Pulsed <sup>b</sup>	-94	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	121	mJ
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> =25°C	42
		T <sub>C</sub> =70°C	27
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	3	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	50	°C/W

# STU437S

## STD437S

Ver 1.0

### ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-32V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA
ON CHARACTERISTICS						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-1	-1.9	-3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =-10V , I <sub>D</sub> =-16A		13	16	m ohm
		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-12A		22	30	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-10V , I <sub>D</sub> =-16A		32		S
DYNAMIC CHARACTERISTICS °						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V f=1.0MHz		2200		pF
C <sub>OSS</sub>	Output Capacitance			244		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			180		pF
SWITCHING CHARACTERISTICS °						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-20V I <sub>D</sub> =-1.0A V <sub>GS</sub> =-10V R <sub>GEN</sub> = 6 ohm		36		ns
t <sub>r</sub>	Rise Time			32		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			109		ns
t <sub>f</sub>	Fall Time			28		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-20V, I <sub>D</sub> =-16A, V <sub>GS</sub> =-10V		37		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-20V, I <sub>D</sub> =-16A,		4.3		nC
Q <sub>gd</sub>	Gate-Drain Charge	V <sub>GS</sub> =-10V		12		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> = -4A		-0.8	-1.3	V
Notes						
a.Surface Mounted on FR4 Board,t ≤ 10sec.						
b.Pulse Test:Pulse Width < 300us, Duty Cycle < 2%.						
c.Guaranteed by design, not subject to production testing.						
d.Starting T <sub>J</sub> =25°C,L=0.5mH,V <sub>DD</sub> = 20V .(See Figure13)						
e.Drain current limited by maximum junction temperature.						

Sep,09,2013

# STU437S STD437S

Ver 1.0

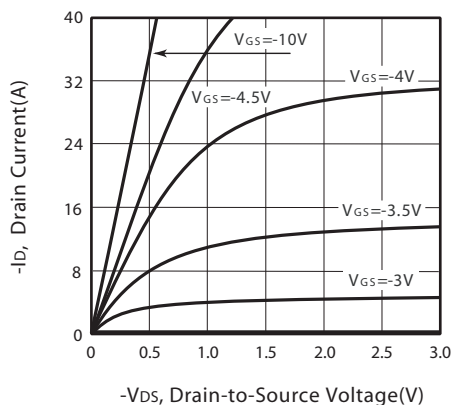


Figure 1. Output Characteristics

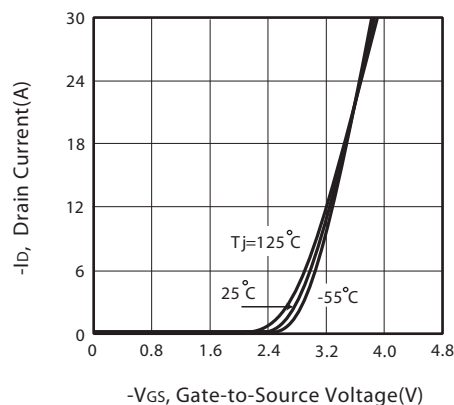


Figure 2. Transfer Characteristics

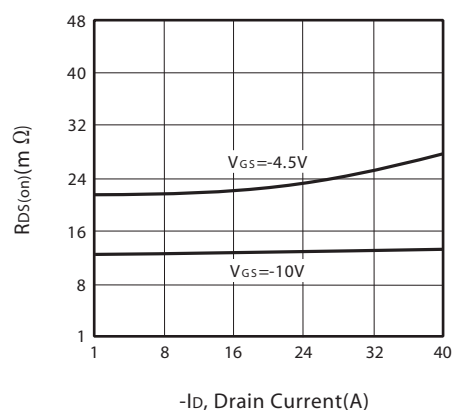


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

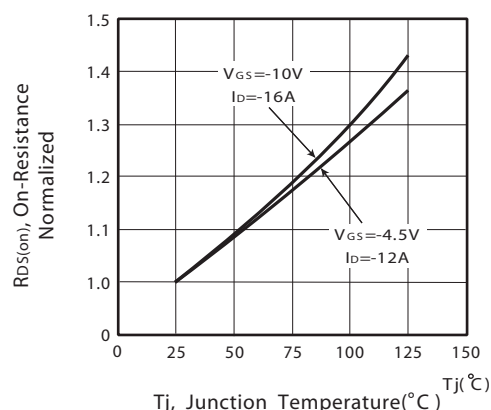


Figure 4. On-Resistance Variation with Drain Current and Temperature

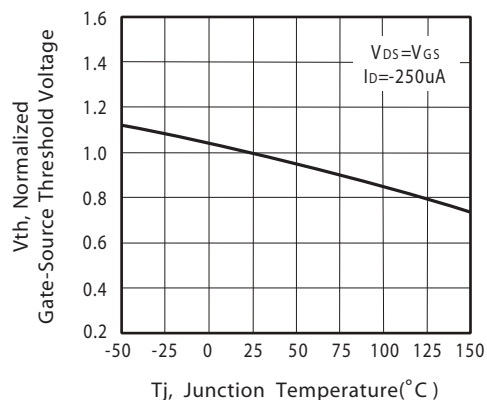


Figure 5. Gate Threshold Variation with Temperature

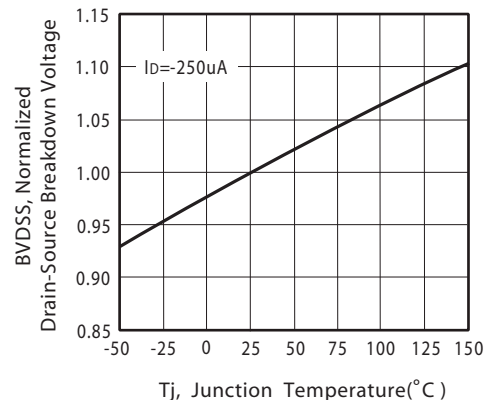


Figure 6. Breakdown Voltage Variation with Temperature

Sep,09,2013

# STU437S STD437S

Ver 1.0

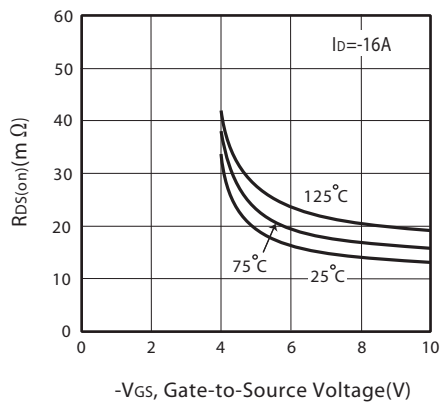


Figure 7. On-Resistance vs. Gate-Source Voltage

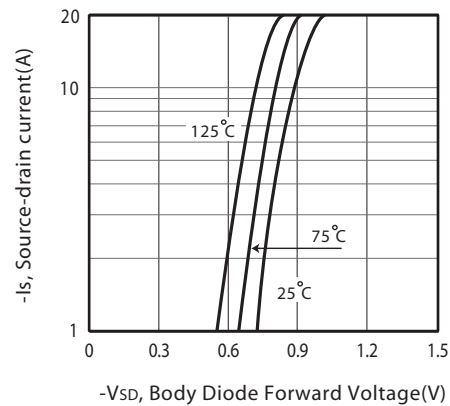


Figure 8. Body Diode Forward Voltage Variation with Source Current

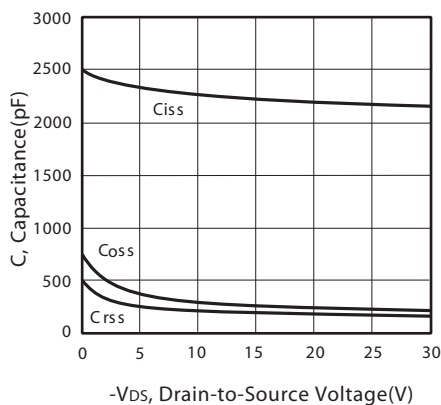


Figure 9. Capacitance

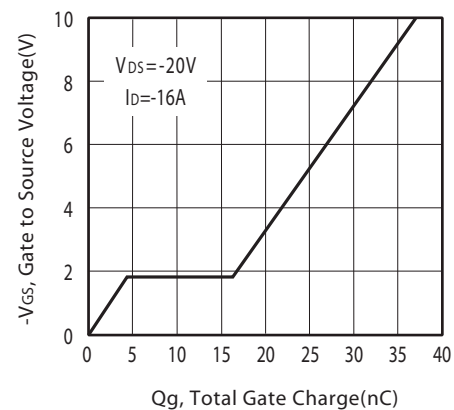


Figure 10. Gate Charge

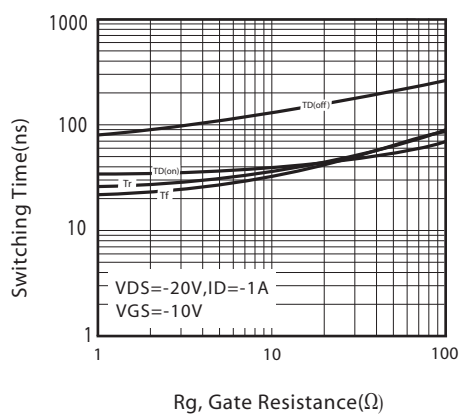


Figure 11. switching characteristics

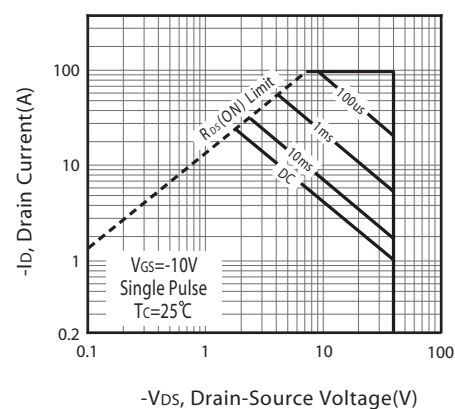
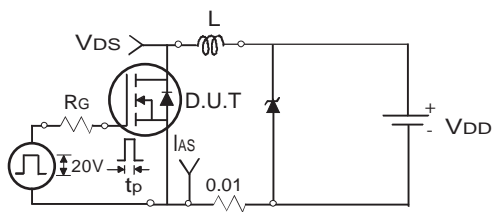


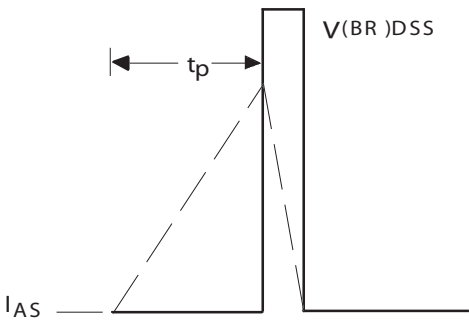
Figure 12. Maximum Safe Operating Area

Sep,09,2013



Uncamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

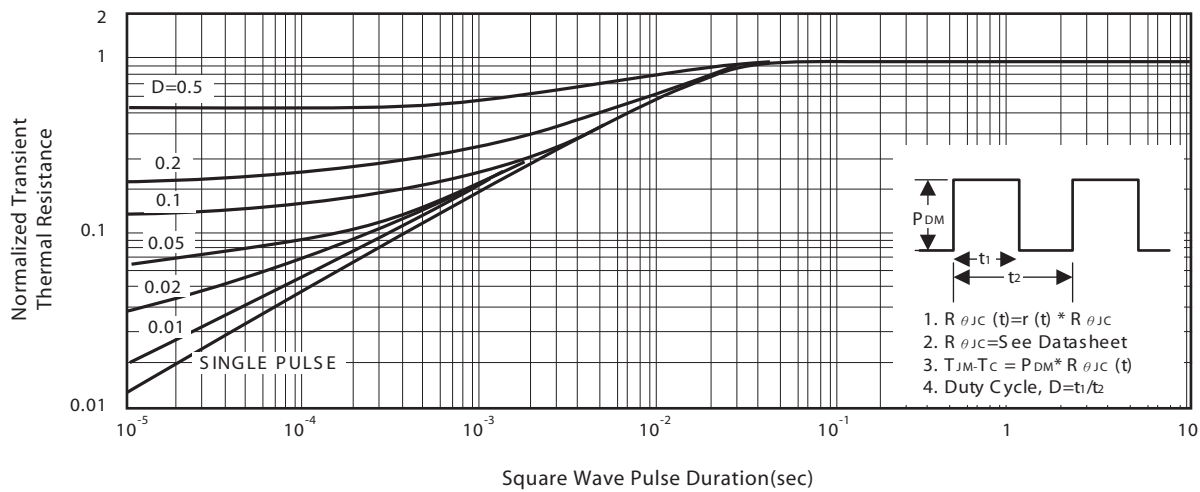


Figure 14. Normalized Thermal Transient Impedance Curve

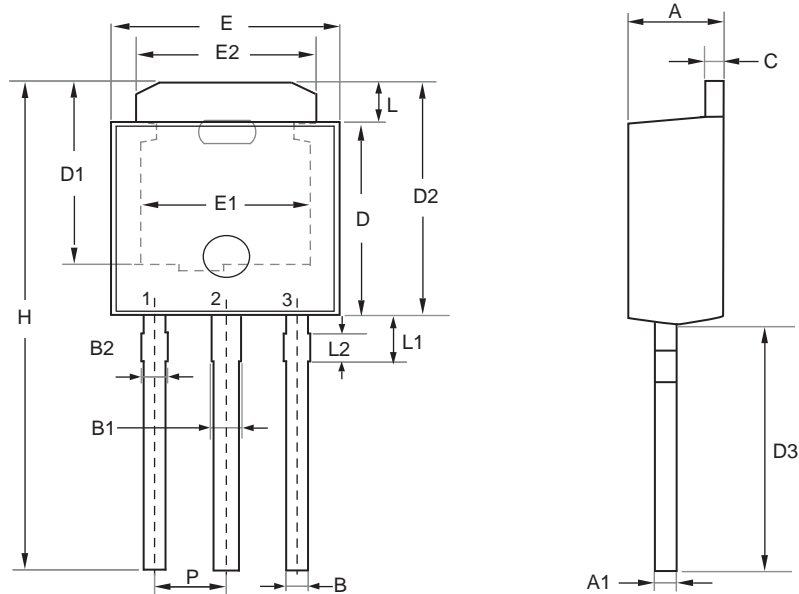
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## STD437S

Ver 1.0

### PACKAGE OUTLINE DIMENSIONS

TO-251



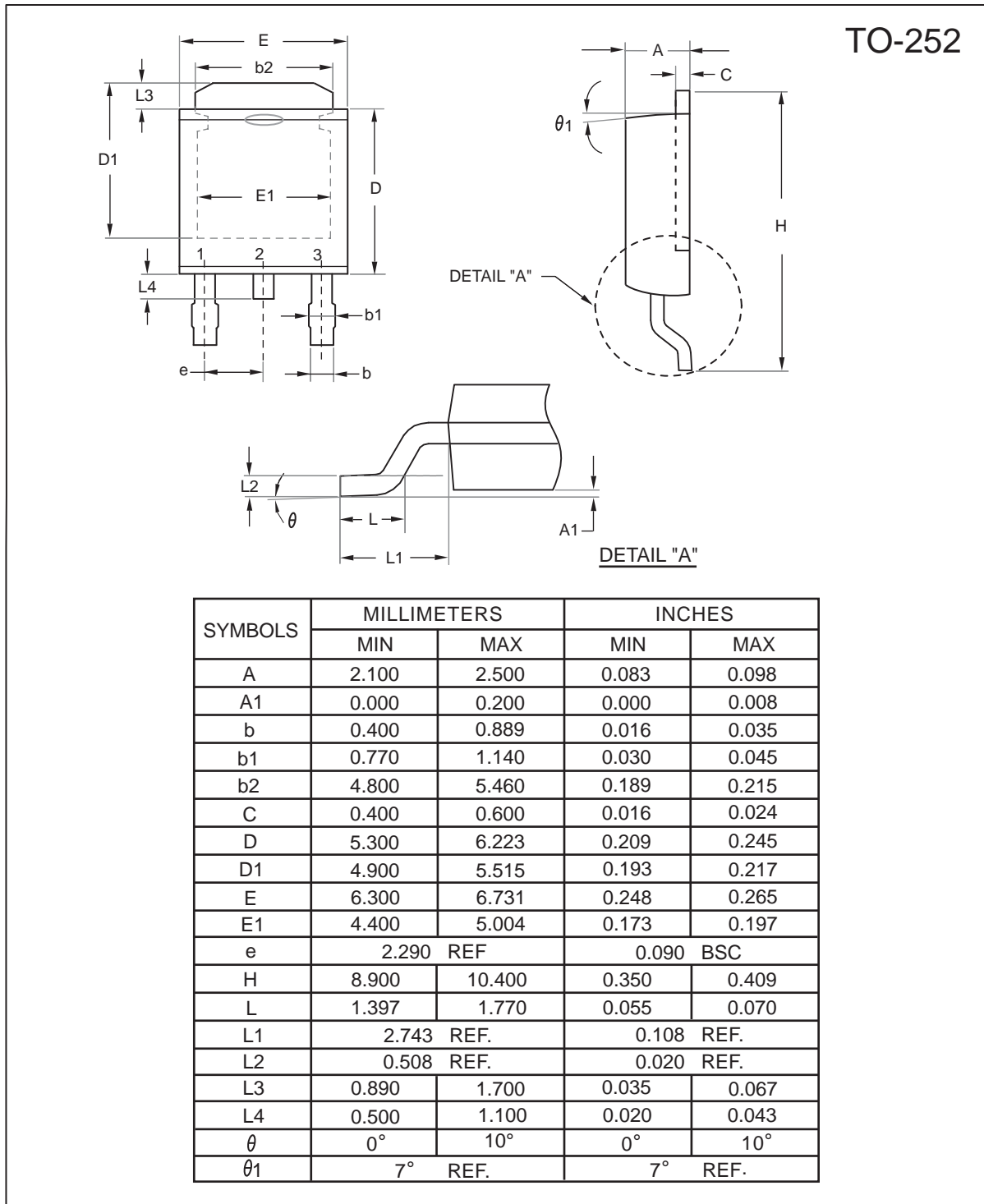
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.100	2.500	0.083	0.098
A1	0.350	0.650	0.014	0.026
B	0.400	0.800	0.016	0.031
B1	0.650	1.050	0.026	0.041
B2	0.500	0.900	0.020	0.035
C	0.400	0.600	0.016	0.024
D	5.300	5.700	0.209	0.224
D1	4.900	5.300	0.193	0.209
D2	6.700	7.300	0.264	0.287
D3	7.000	8.000	0.276	0.315
H	10.830	11.430	0.426	0.450
E	6.300	6.700	0.248	0.264
E1	4.600	4.900	0.181	0.193
E2	4.800	5.200	0.189	0.205
L	1.300	1.700	0.051	0.067
L1	1.400	1.800	0.055	0.071
L2	0.500	0.900	0.020	0.035
P	2.300 BSC		0.091 BSC	

Sep,09,2013

# STU437S

## STD437S

Ver 1.0



Sep,09,2013

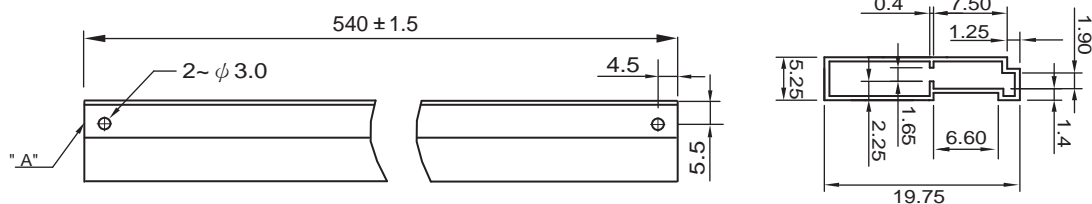
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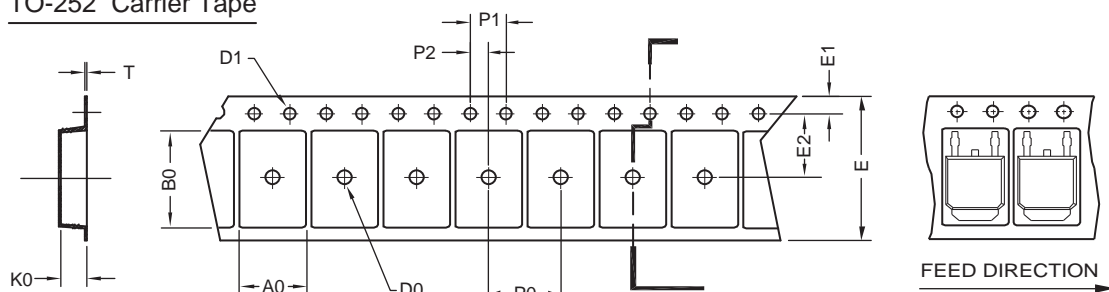
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### TO-251 Tube/TO-252 Tape and Reel Data

#### TO-251 Tube



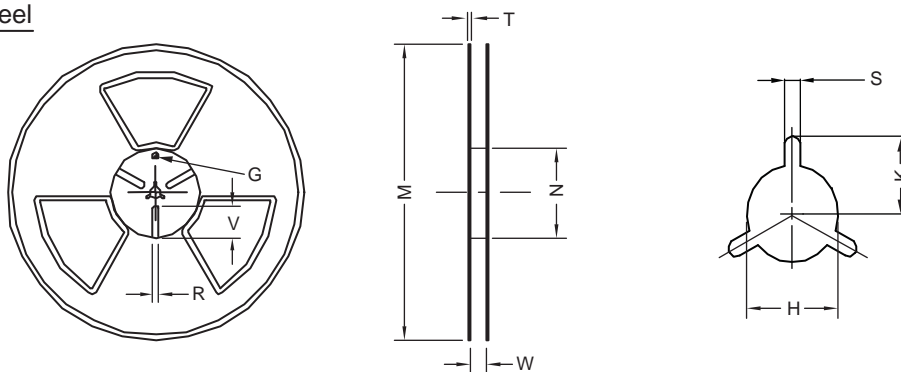
#### TO-252 Carrier Tape



UNIT:mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TO-252 (16 mm)	6.96 ±0.1	10.49 ±0.1	2.79 ±0.1	φ 2	φ 1.5 + 0.1 - 0	16.0 ±0.3	1.75 ±0.1	7.5 ±0.15	8.0 ±0.1	4.0 ±0.1	2.0 ±0.15	0.3 ±0.05

#### TO-252 Reel



UNIT:mm

TAPE SIZE	REEL SIZE	M	N	W	T	H	K	S	G	R	V
16 mm	φ 330	φ 330 ± 0.5	φ 97 ± 1.0	17.0 + 1.5 - 0	2.2	φ 13.0 + 0.5 - 0.2	10.6	2.0 ±0.5	---	---	---

Sep,09,2013



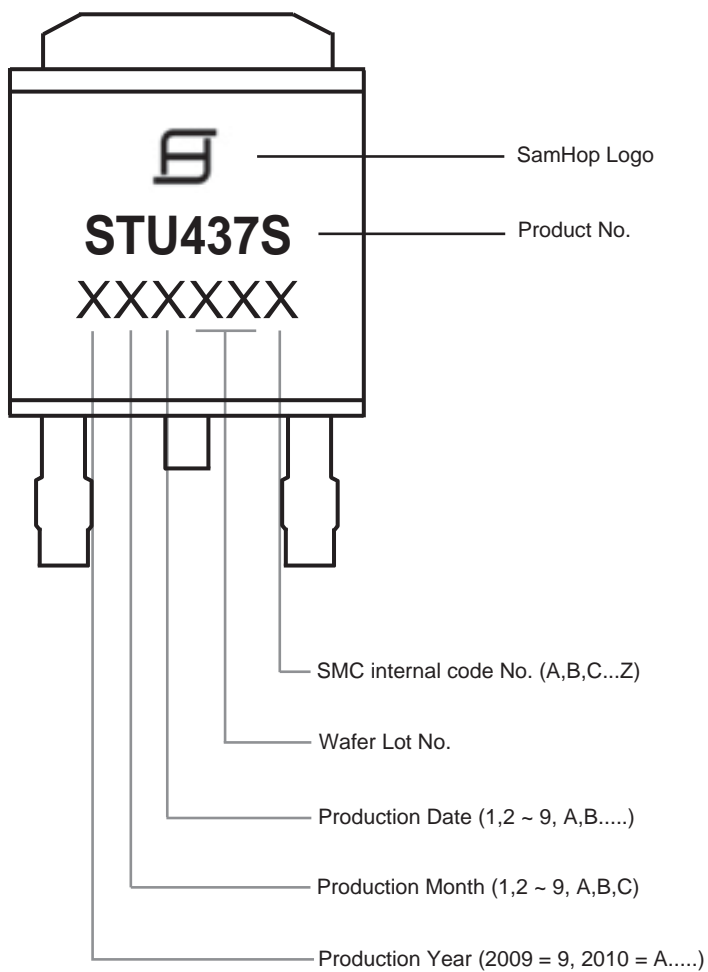
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Ver 1.0

### TOP MARKING DEFINITION

TO-252



Sep,09,2013

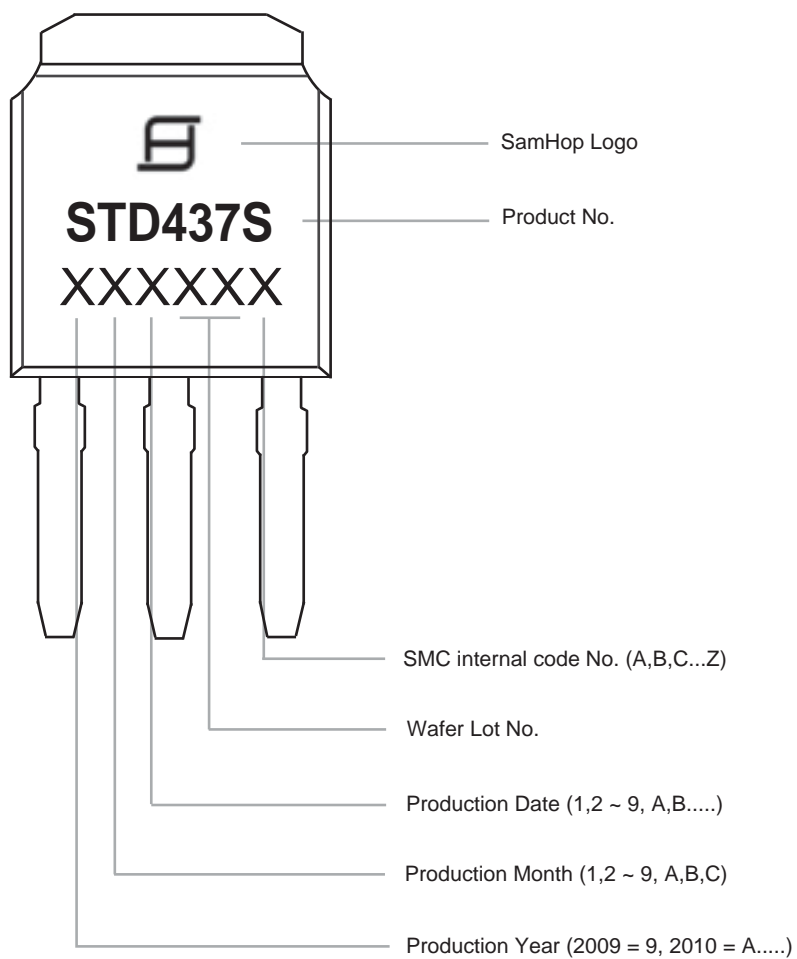
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Ver 1.0

### TOP MARKING DEFINITION

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Sep,09,2013