



## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

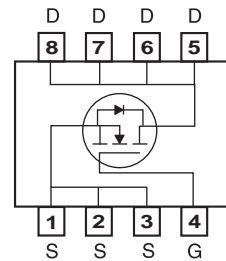
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
80V	80A	5.5 @ V <sub>GS</sub> =10V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.

**DFN 5x6**

PIN1



### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter		Limit	Units
V <sub>DS</sub>	Drain-Source Voltage		80	V
V <sub>GS</sub>	Gate-Source Voltage		±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>c</sup>	T <sub>C</sub> =25°C	80	A
		T <sub>C</sub> =70°C	64	A
I <sub>DM</sub>	-Pulsed <sup>a c</sup>		163	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>		930	mJ
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> =25°C	83	W
		T <sub>C</sub> =70°C	53	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range		-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	1.5	°C/W
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# SP823C

Ver 1.0

## ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	80			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =64V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA
ON CHARACTERISTICS						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2	3	4	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =20A		4.2	5.5	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V , I <sub>D</sub> =20A		72		S
DYNAMIC CHARACTERISTICS <sup>b</sup>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		3745		pF
C <sub>oss</sub>	Output Capacitance			624		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			418		pF
SWITCHING CHARACTERISTICS <sup>b</sup>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =40V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> = 6 ohm		87		ns
t <sub>r</sub>	Rise Time			146		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			119		ns
t <sub>f</sub>	Fall Time			54		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =40V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V		58		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =40V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V		7		nC
Q <sub>gd</sub>	Gate-Drain Charge			26		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =18A		0.76	1.3	V
Notes						
a. Pulse Test: Pulse Width ≤ 10us, Duty Cycle ≤ 1%.						
b. Guaranteed by design, not subject to production testing.						
c. Drain current limited by maximum junction temperature.						
d. Starting T <sub>J</sub> =25°C, L=0.5mH, V <sub>DD</sub> = 40V. (See Figure13)						
e. Mounted on FR4 Board of 1 inch <sup>2</sup> , 2oz.						

Aug,27,2015

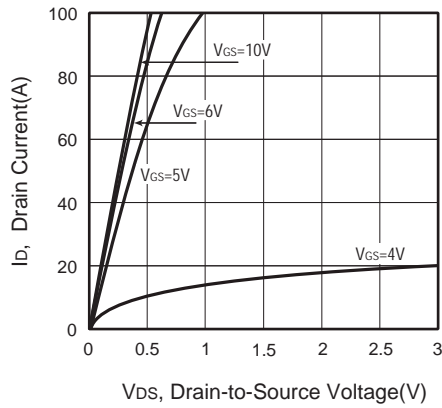


Figure 1. Output Characteristics

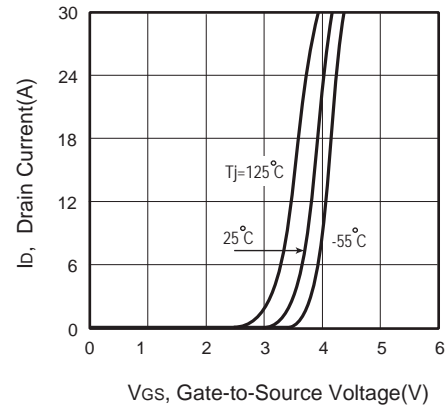


Figure 2. Transfer Characteristics

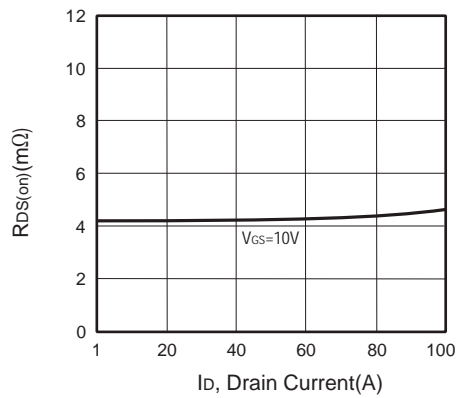


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

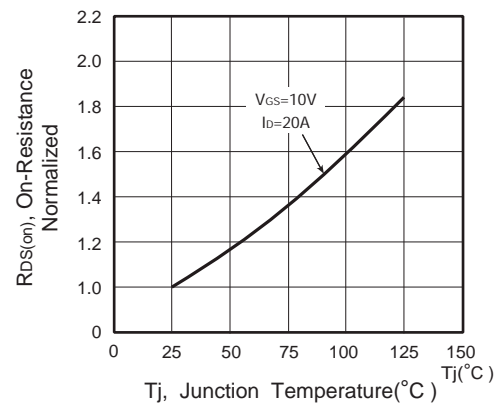


Figure 4. On-Resistance Variation with Drain Current and Temperature

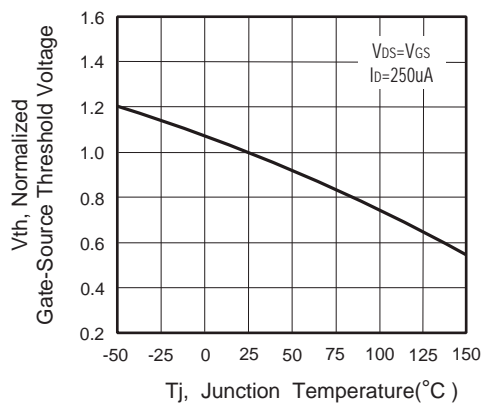


Figure 5. Gate Threshold Variation with Temperature

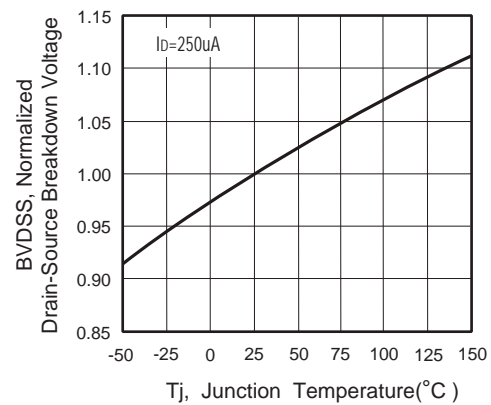


Figure 6. Breakdown Voltage Variation with Temperature

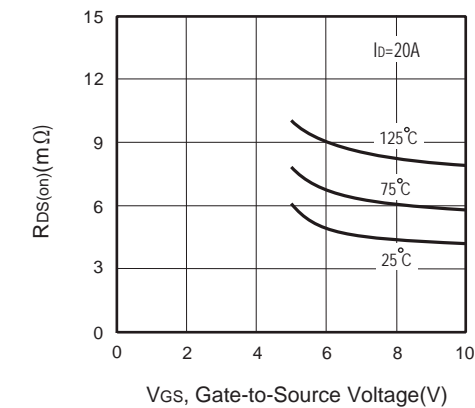


Figure 7. On-Resistance vs. Gate-Source Voltage

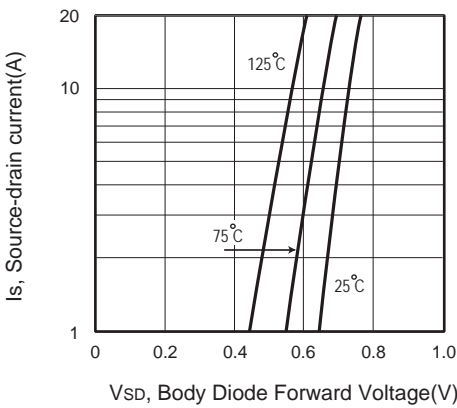


Figure 8. Body Diode Forward Voltage Variation with Source Current

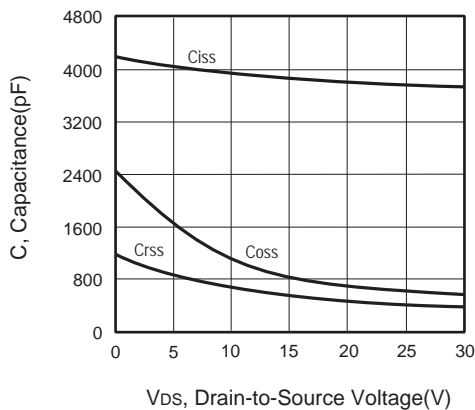


Figure 9. Capacitance

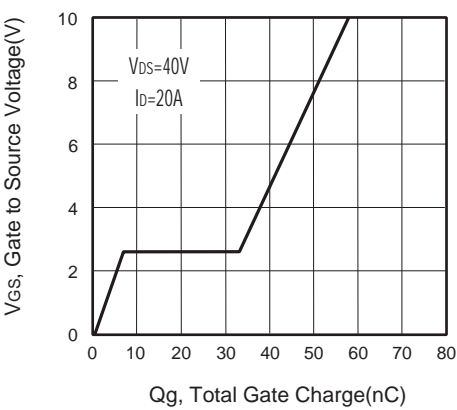


Figure 10. Gate Charge

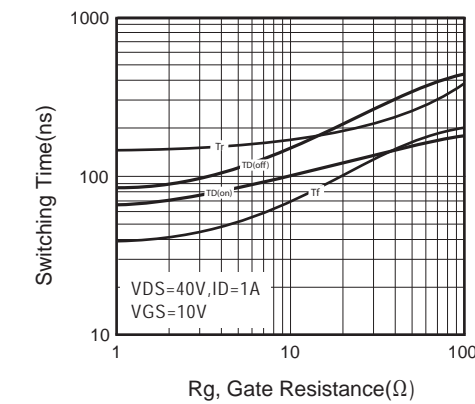


Figure 11. switching characteristics

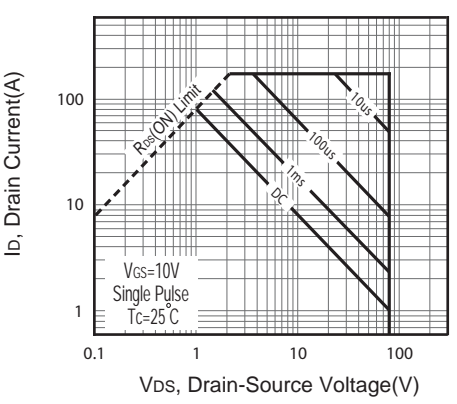
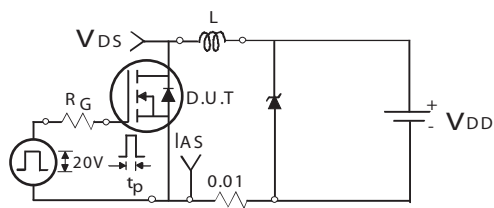
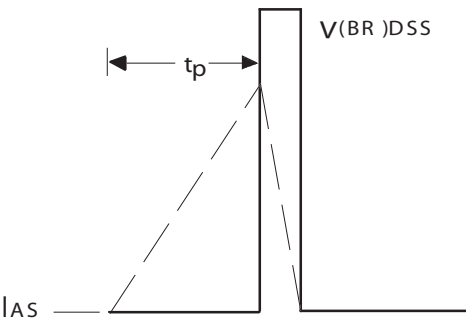


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

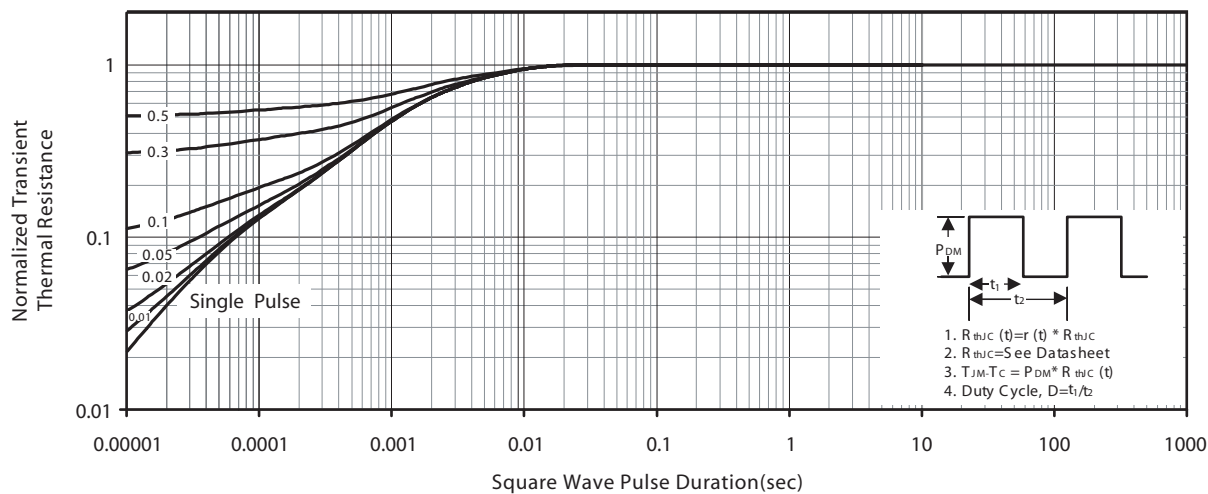
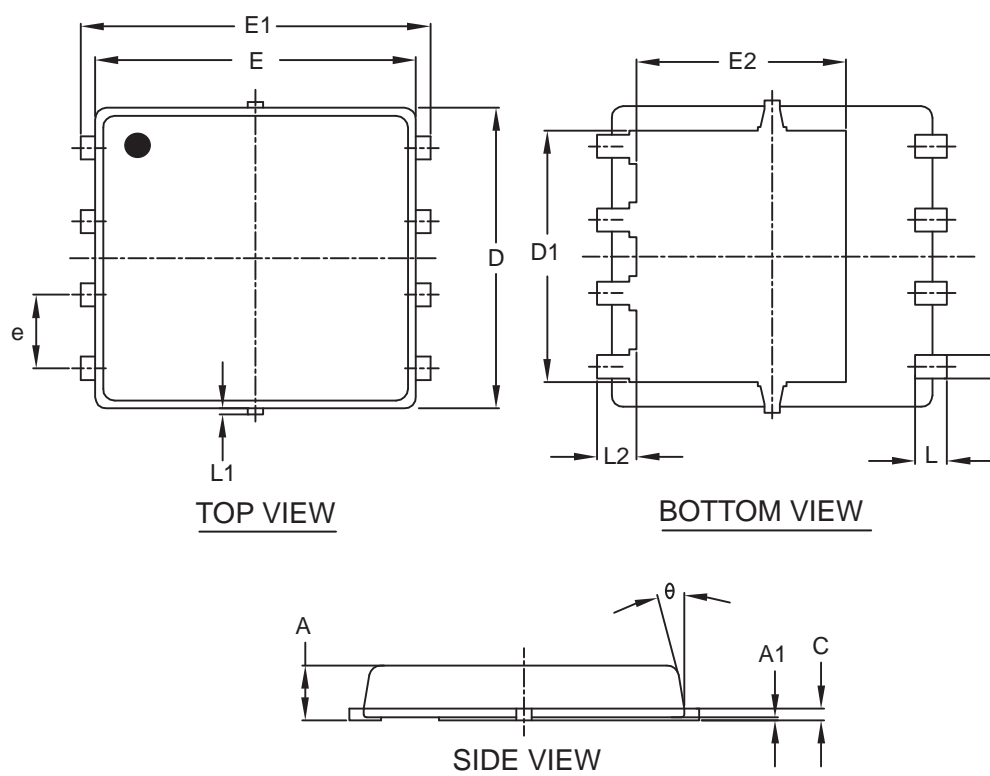


Figure 14. Normalized Thermal Transient Impedance Curve

## PACKAGE OUTLINE DIMENSIONS

## DFN 5x6-8L



SYMBOLS	MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.95	1.00
A1	0.00	—	0.05
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	5.20 BSC		
D1	4.35 BSC		
E	5.55 BSC		
E1	6.05 BSC		
E2	3.62 BSC		
e	1.27 BSC		
L	0.45	0.55	0.65
L1	0.00	—	0.15
L2	0.68 REF		
$\theta$	0°	—	10°

## TOP MARKING DEFINITION

