



Dual N-Channel Enhancement Mode Field Effect Transistor

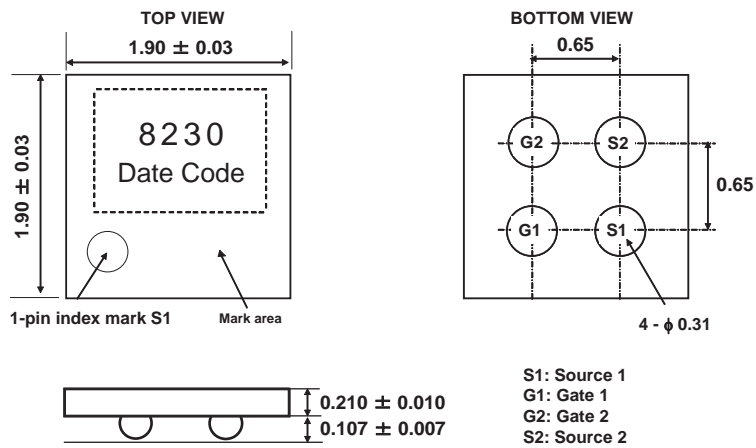
PRODUCT SUMMARY

V _{SSS}	I _S	R _{DS(ON)} (mΩ) Max
20V	8A	19.0 @ V _{GS} =4.5V
		20.0 @ V _{GS} =4.0V
		21.0 @ V _{GS} =3.1V
		30.0 @ V _{GS} =2.5V

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.

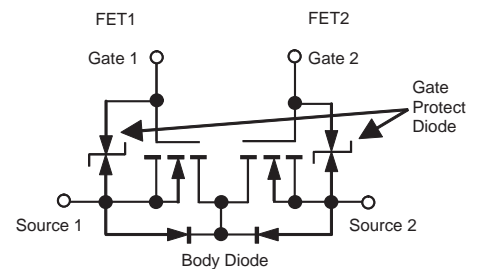
WLCSP



Unit : mm

ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Symbol	Parameter	Limit	Units
V _{SSS}	Source-Source Voltage	20	V
V _{GSS}	Gate-Source Voltage	±12	V
I _S	Source Current-Continuous ^a	8	A
I _{SP}	-Pulsed ^b	80	A
P _T	Total Power Dissipation ^a	1.6	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C



SC8230

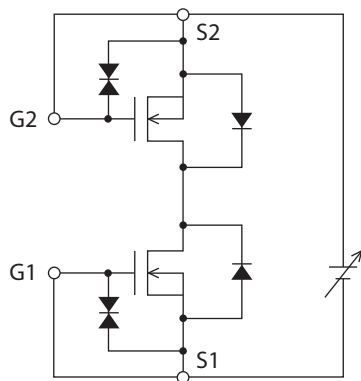
Ver 4.0

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

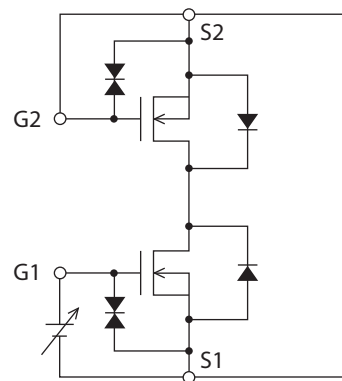
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{SSS}	Source-Source Breakdown Voltage	V _{GS} =0V, I _S =250uA	20			V
I _{SSS}	Zero Gate Voltage Source Current	V _{SS} =20V, V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±8V, V _{SS} =0V			±1	uA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{SS} =V _{GS} , I _S =250uA	0.5	0.7	1.5	V
R _{SS(ON)}	Source-Source On-State Resistance	V _{GS} =4.5V, I _S =4A	9.5	15.0	19.0	m ohm
		V _{GS} =4.0V, I _S =4A	10.0	16.0	20.0	m ohm
		V _{GS} =3.1V, I _S =4A	11.0	17.5	21.0	m ohm
		V _{GS} =2.5V, I _S =4A	13.0	23.0	30.0	m ohm
g _{FS}	Forward Transconductance	V _{SS} =5V, I _S =4A		24		S
SWITCHING CHARACTERISTICS ^c						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =20V I _S =4A V _{GS} =4.0V R _{GEN} =6 ohm		203		ns
t _r	Rise Time			893		ns
t _{D(OFF)}	Turn-Off Delay Time			1910		ns
t _f	Fall Time			1900		ns
Q _g	Total Gate Charge	V _{DD} =20V, I _S =8A, V _{G1S1} =4.0V		16.6		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V _{FSS}	Diode Forward Voltage	V _{GS} =0V, I _S =1.5A		0.77	1.2	V
Note a. Mounted on FR4 board of 25.4mm x 25.4mm x 1.6mm. b. Pulse Test: Pulse Width < 10us, Duty Cycle < 1%. c. Guaranteed by design, not subject to production testing.						

Sep,04,2015

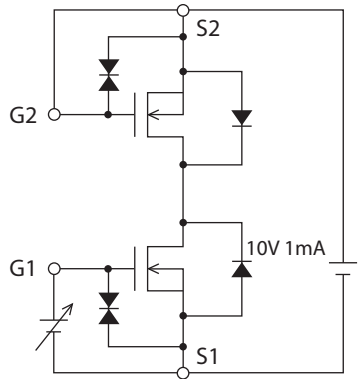
V_{SSS} / I_{SSS}



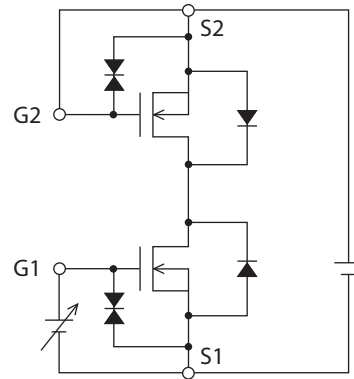
$I_{GSS} (+) / (-)$



$V_{GS} (off)$

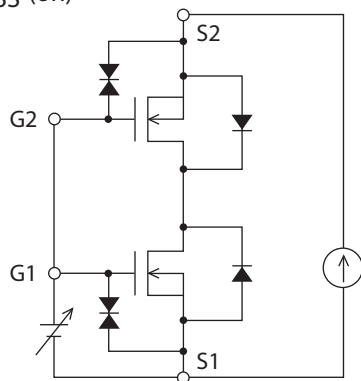


$|y_{fs}|$

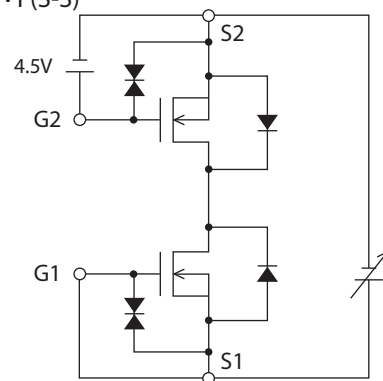


* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

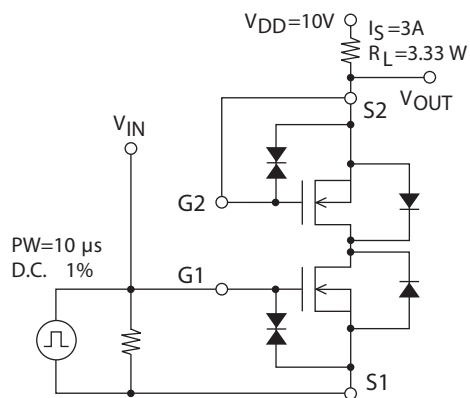
$R_{SS} \text{ (on)}$



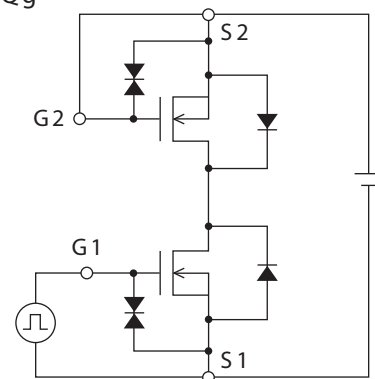
$V_F(S-S)$



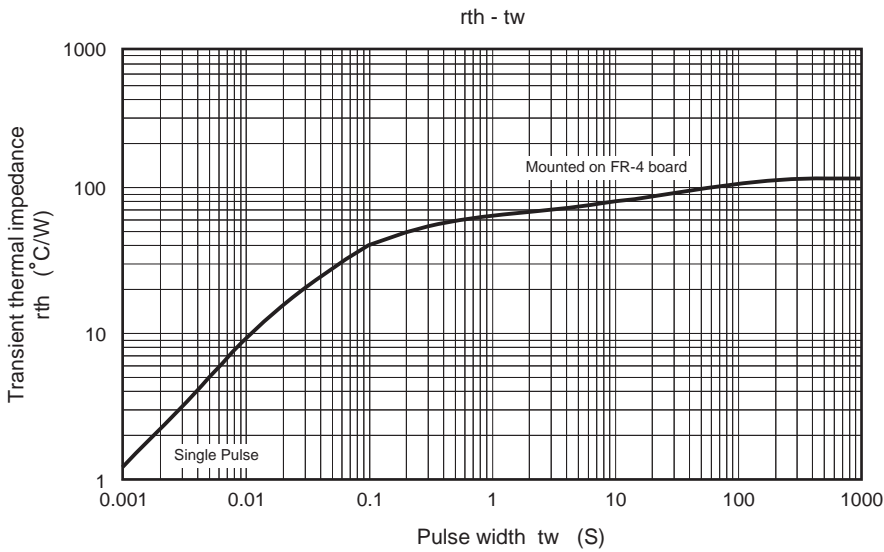
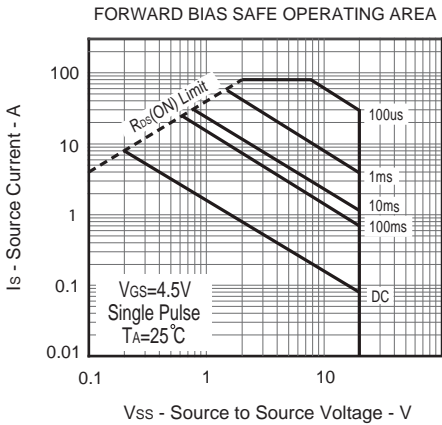
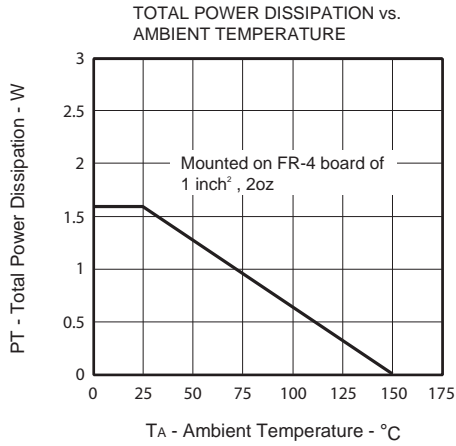
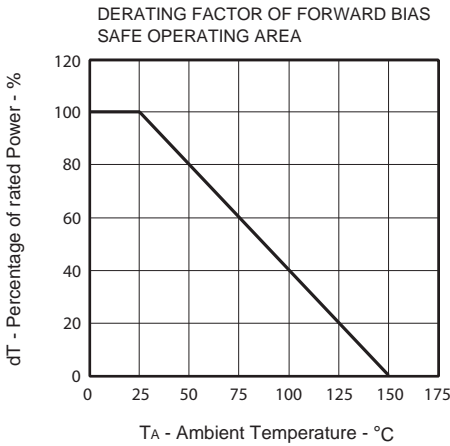
$t_d(\text{on}), t_r, t_d(\text{off}), t_f$

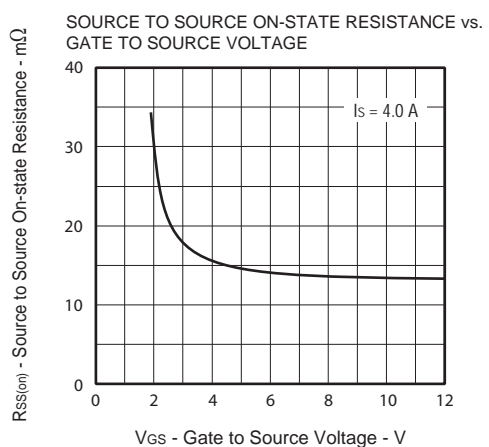
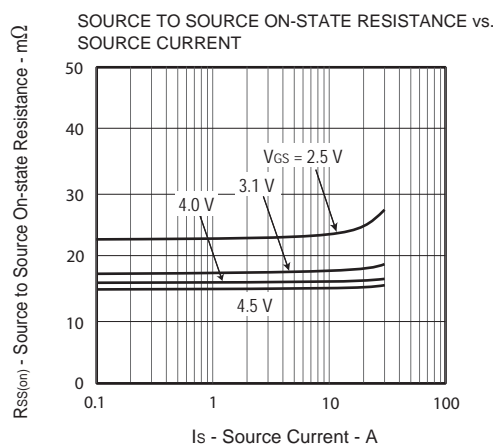
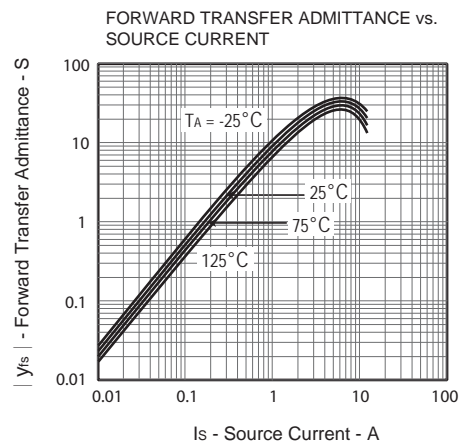
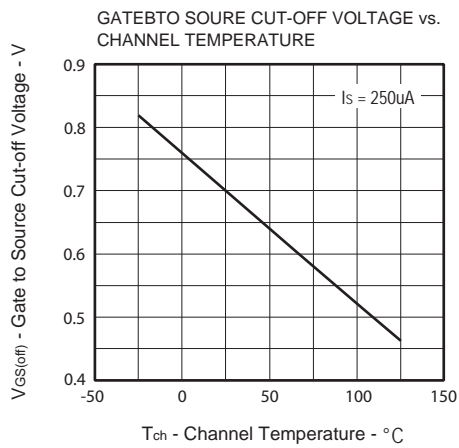
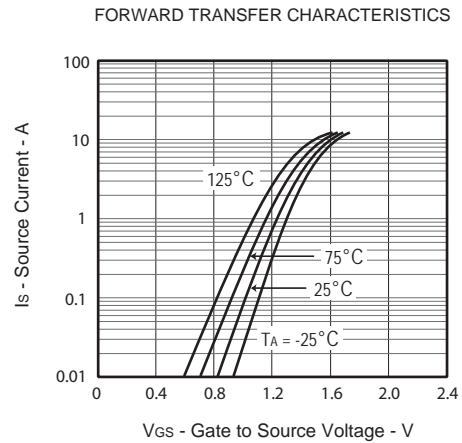
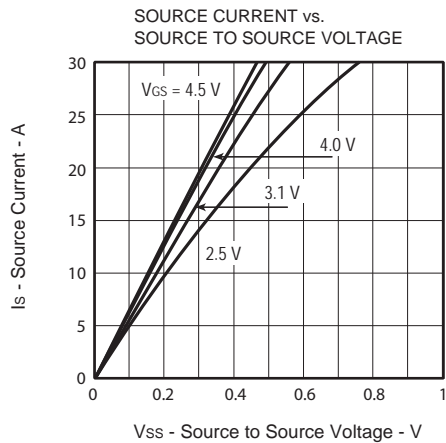


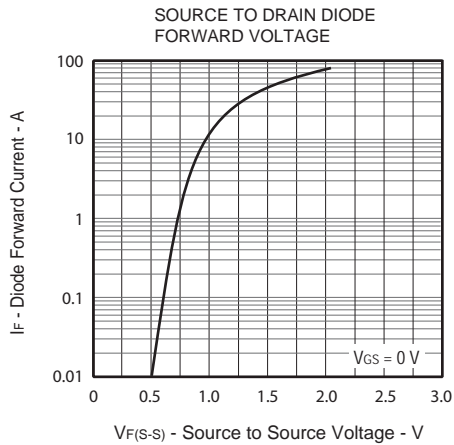
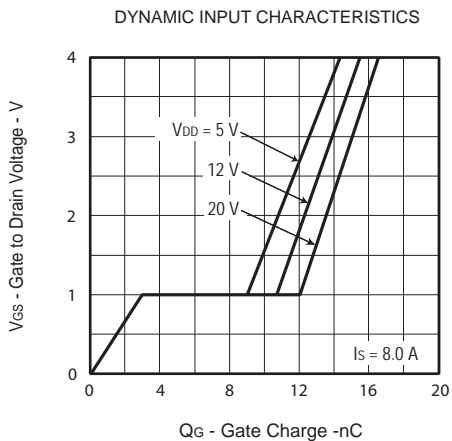
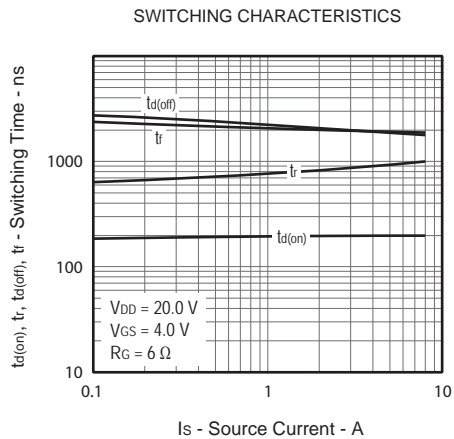
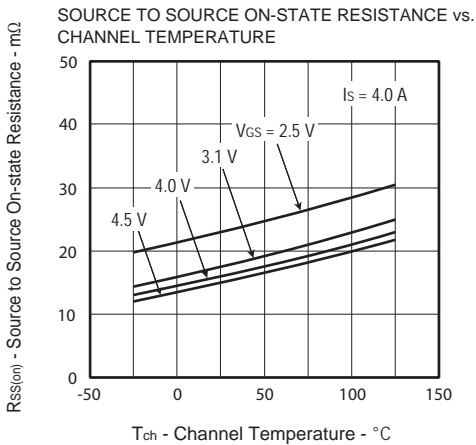
Q_g



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TOP MARKING DEFINITION

WLCSP

