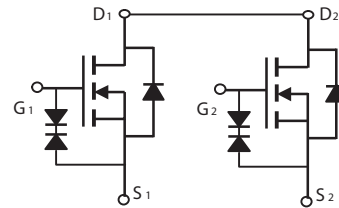
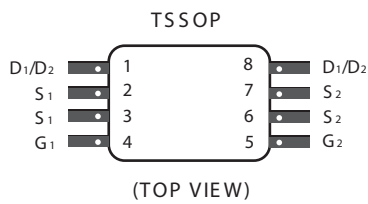


**Dual N-Channel Enhancement Mode Field Effect Transistor****PRODUCT SUMMARY**

V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
20V	7A	18.5 @ V <sub>GS</sub> =4.5V
		19.5 @ V <sub>GS</sub> =4.0V
		20.0 @ V <sub>GS</sub> =3.7V
		23.0 @ V <sub>GS</sub> =3.1V
		28.5 @ V <sub>GS</sub> =2.5V

**FEATURES**

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.
- ESD HBM > 2KV.

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	20	V
V <sub>GS</sub>	Gate-Source Voltage	±12	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>A</sub> =25°C	7.0
		T <sub>A</sub> =70°C	5.6
I <sub>DM</sub>	-Pulsed <sup>b</sup>	28	A
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> =25°C	1.5
		T <sub>A</sub> =70°C	1
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

**THERMAL CHARACTERISTICS**

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	85	°C/W
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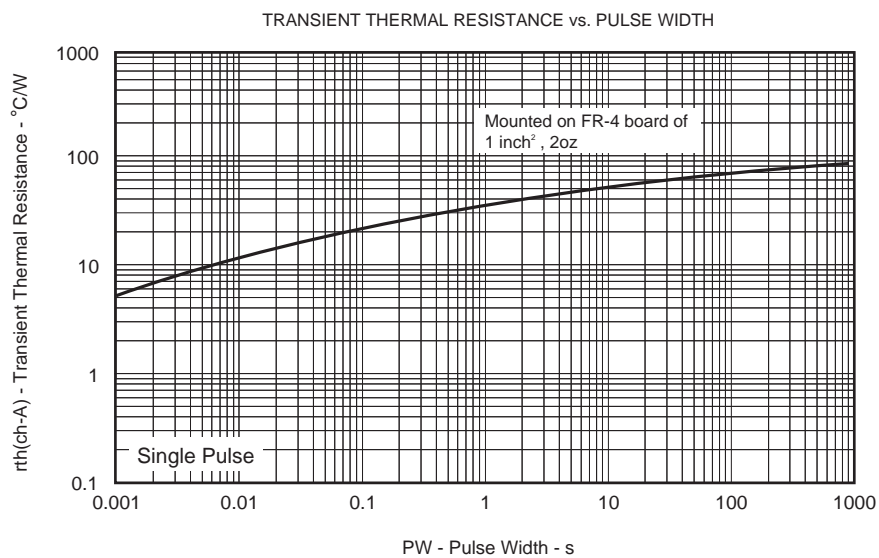
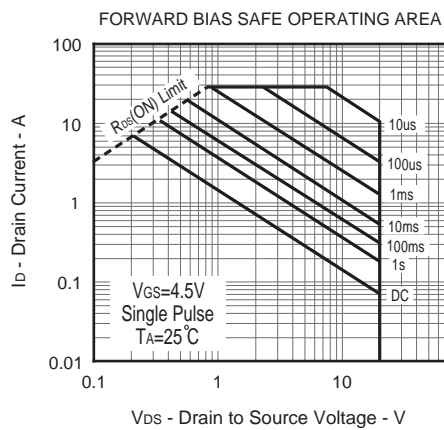
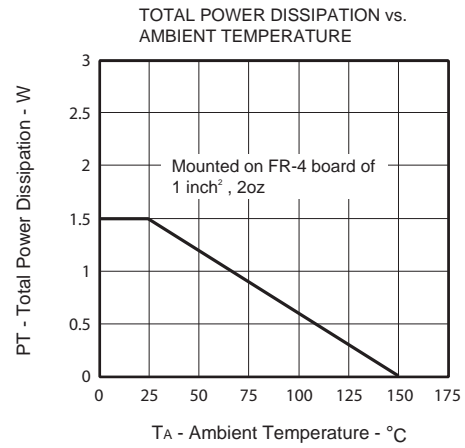
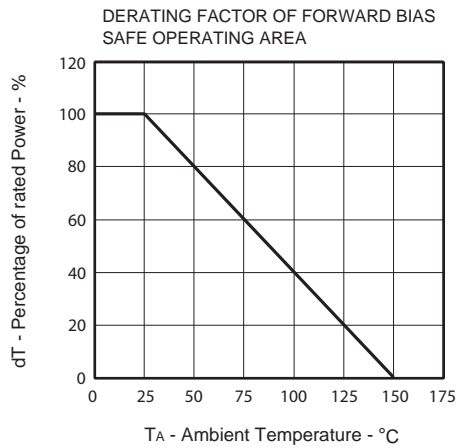
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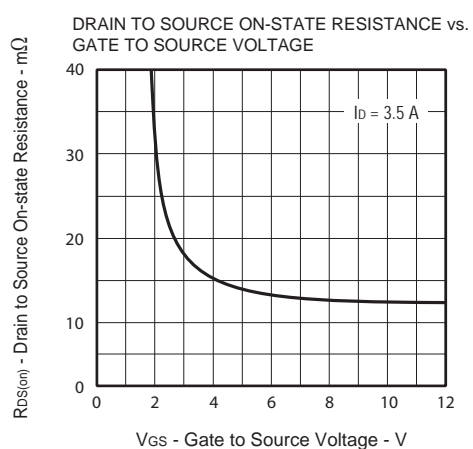
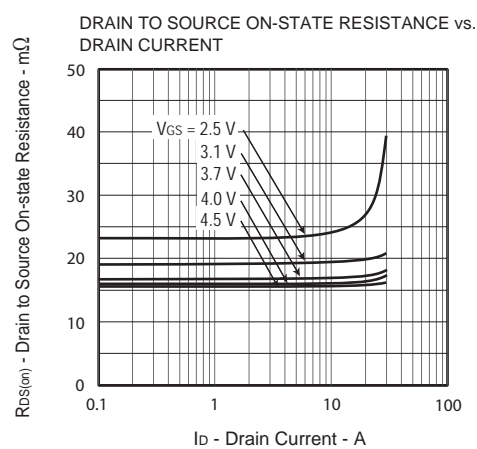
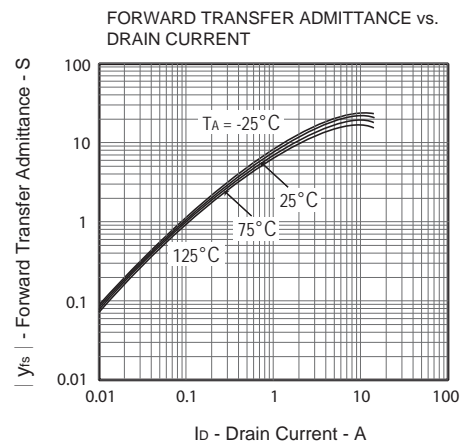
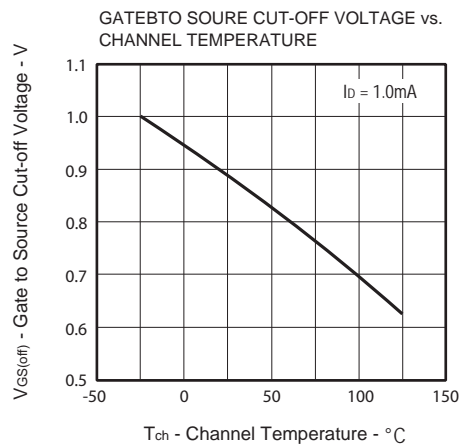
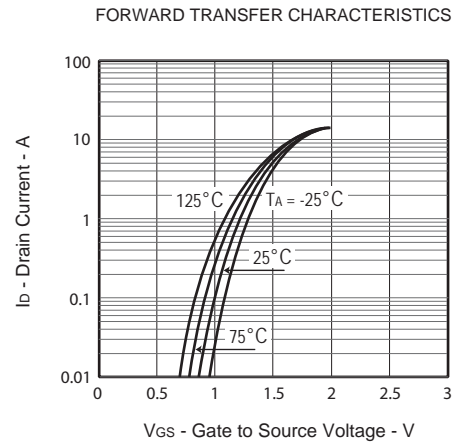
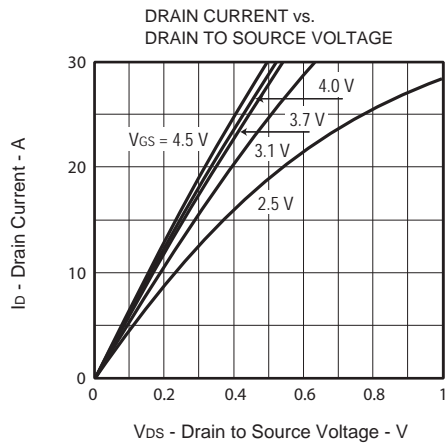
Ver 2.0

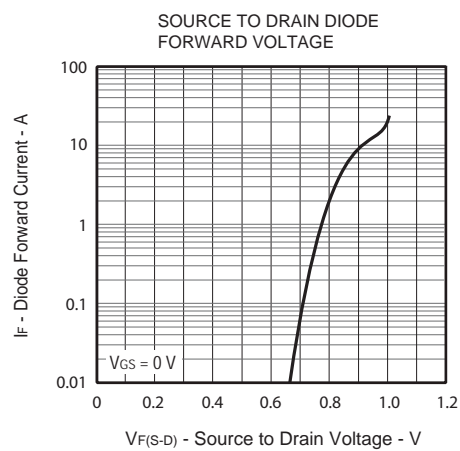
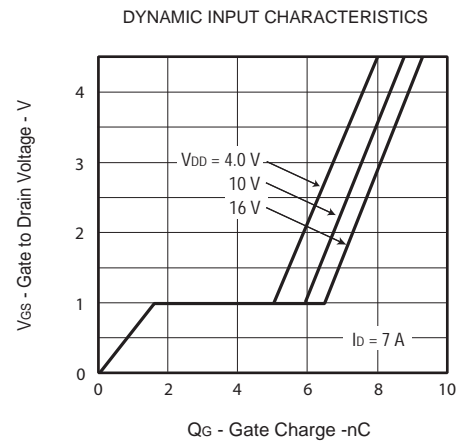
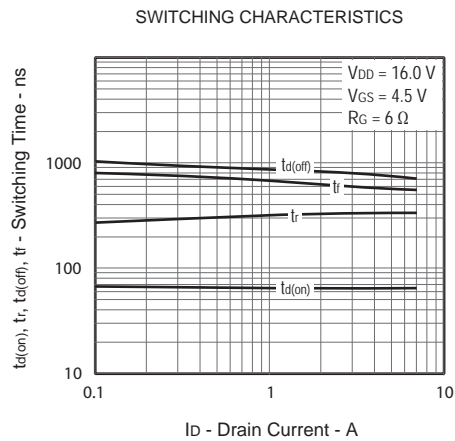
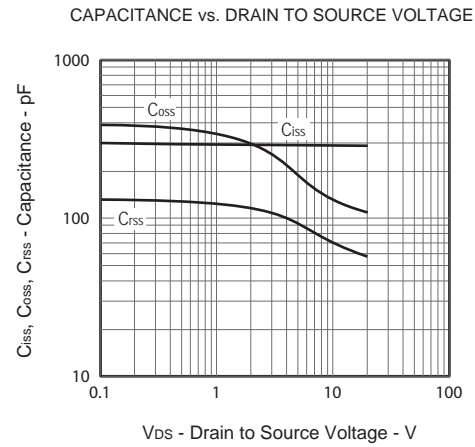
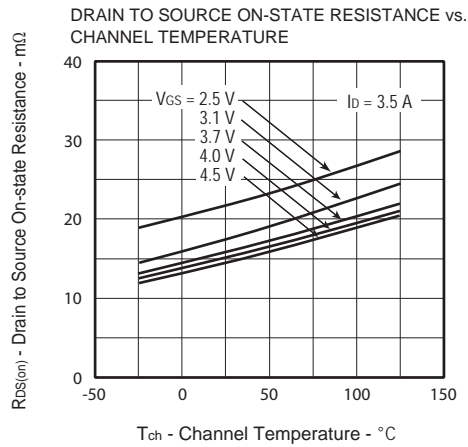
## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =16V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±12V , V <sub>DS</sub> =0V			±10	uA
ON CHARACTERISTICS						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =1mA	0.5	0.9	1.5	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =4.5V , I <sub>D</sub> =3.5A	14.0	16.5	18.5	m ohm
		V <sub>GS</sub> =4.0V , I <sub>D</sub> =3.5A	14.5	17.0	19.5	m ohm
		V <sub>GS</sub> =3.7V , I <sub>D</sub> =3.5A	15.0	17.5	20.0	m ohm
		V <sub>GS</sub> =3.1V , I <sub>D</sub> =3.5A	16.0	19.5	23.0	m ohm
		V <sub>GS</sub> =2.5V , I <sub>D</sub> =3.5A	18.0	23.5	28.5	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =3.5A		19		S
DYNAMIC CHARACTERISTICS °						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =10V,V <sub>GS</sub> =0V f=1.0MHz		300		pF
C <sub>OSS</sub>	Output Capacitance			151		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			71		pF
SWITCHING CHARACTERISTICS °						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =16V I <sub>D</sub> =3.5A V <sub>GS</sub> =4.5V R <sub>GEN</sub> = 6 ohm		61		ns
t <sub>r</sub>	Rise Time			295		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			821		ns
t <sub>f</sub>	Fall Time			580		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =16V,I <sub>D</sub> =7A, V <sub>GS</sub> =4.5V		9		nC
Q <sub>gs</sub>	Gate-Source Charge			1.5		nC
Q <sub>gd</sub>	Gate-Drain Charge			5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V,I <sub>S</sub> =1.0A		0.78	1.2	V
Notes						
a.Surface Mounted on FR4 Board,t < 10sec.						
b.Pulse Test:Pulse Width < 10us, Duty Cycle < 1%.						
c.Guaranteed by design, not subject to production testing.						

May,20,2011

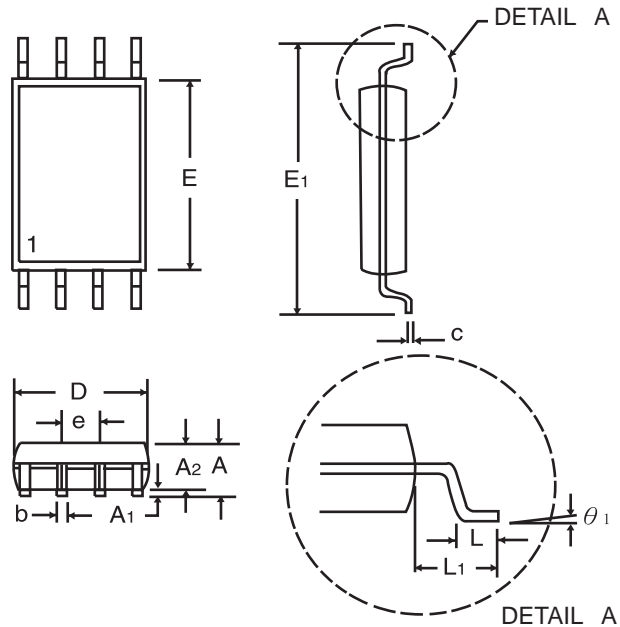






## PACKAGE OUTLINE DIMENSIONS

### TSSOP-8

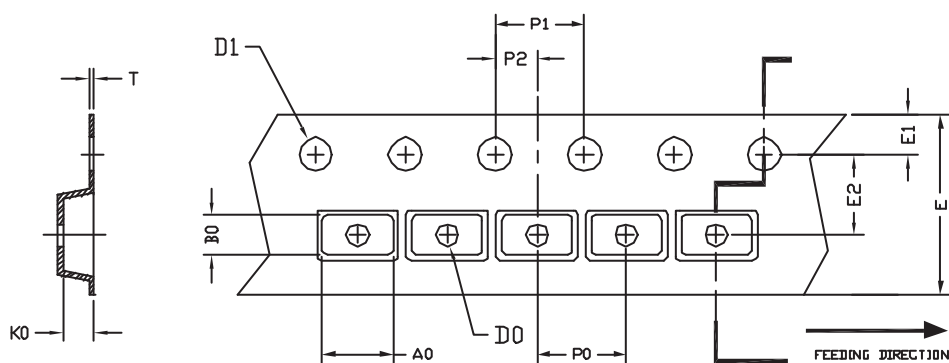


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	1.20	0.033	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.127		0.005	
D	2.90	3.10 <sup>②</sup>	0.114	0.122 <sup>②</sup>
E	4.30	4.50 <sup>③</sup>	0.169	0.177 <sup>③</sup>
E1	6.20	6.60	0.244	0.260
e	0.65BSC		0.025BSC	
L	0.50	0.70	0.020	0.028
L1	1.00		0.039	
$\theta_1$	0°	8°	0°	8°

- Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E to be determined at Datum Plane H.

## TSSOP-8 Tape and Reel Data

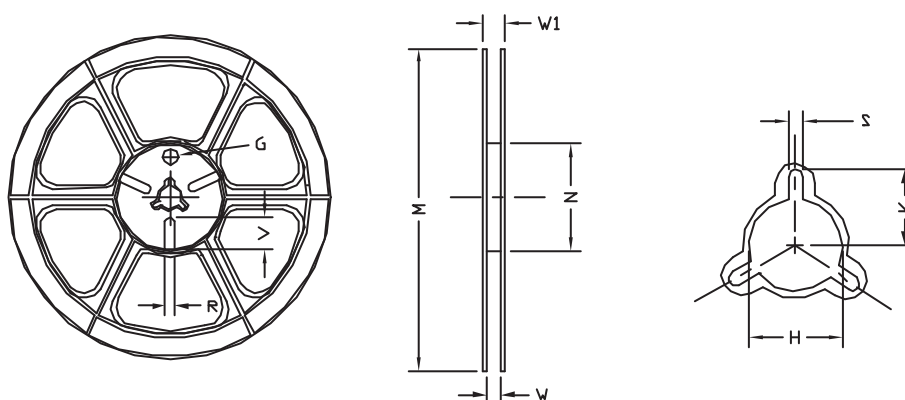
### TSSOP-8 Carrier Tape



UNIT : mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TSSOP 8	6.08	4.40	1.60	$\phi 1.50$ + 0.1 - 0.0	$\phi 1.50$ + 0.1 - 0.0	12.00 $\pm 0.3$	1.75	5.50 $\pm 0.05$	8.00	4.00	2.00 $\pm 0.05$	0.30 $\pm 0.05$

### TSSOP-8 Reel



UNIT : mm

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	$\phi 330$	330	100	12.5	16.0	$\phi 13.0$ + 0.5 - 0.2	10.6	2.0 $\pm 0.5$	---	---	---