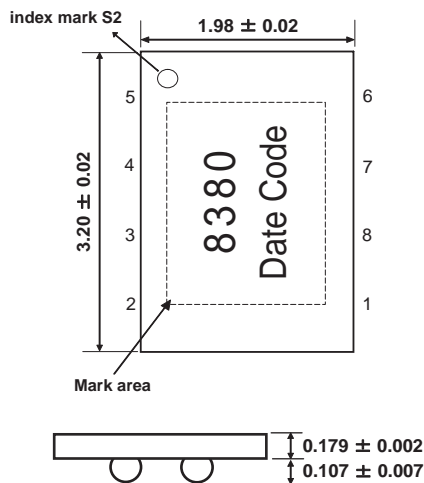
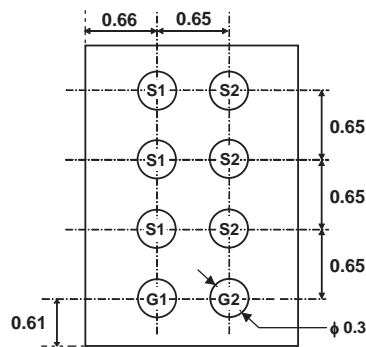


**Dual N-Channel Enhancement Mode Field Effect Transistor****PRODUCT SUMMARY**

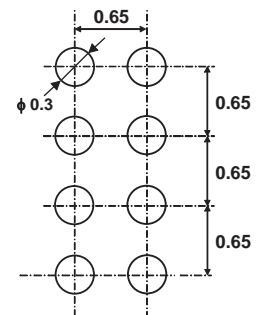
V <sub>SSS</sub>	I <sub>S</sub>	R <sub>SS(ON)</sub> (mΩ) Max
30V	9A	8 @ V <sub>GS</sub> =10V
		13 @ V <sub>GS</sub> =4.5V

**FEATURES**

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.

**WLCSP****TOP VIEW****BOTTOM VIEW**

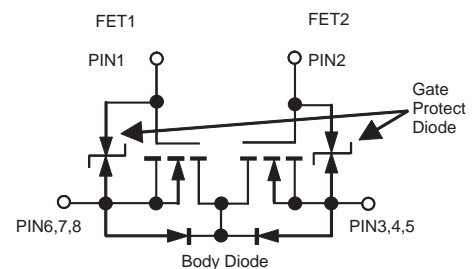
PIN6 : Source 1-1 PIN5 : Source 2-1  
 PIN7 : Source 1-2 PIN4 : Source 2-2  
 PIN8 : Source 1-3 PIN3 : Source 2-3  
 PIN1 : Gate 1 PIN2 : Gate 2

**LAND PATTERN (REFERENCE)**

Unit : mm

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C)**

Symbol	Parameter	Limit	Units
V <sub>SSS</sub>	Source-Source Voltage	30	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>S</sub>	Source Current-Continuous <sup>a</sup>	9	A
I <sub>SP</sub>	-Pulsed <sup>b</sup>	90	A
P <sub>T</sub>	Total Power Dissipation <sup>a</sup>	0.4	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

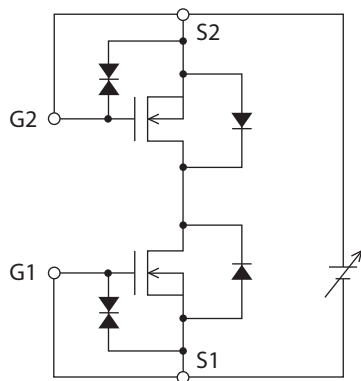


PIN6 : Source 1-1 PIN5 : Source 2-1  
 PIN7 : Source 1-2 PIN4 : Source 2-2  
 PIN8 : Source 1-3 PIN3 : Source 2-3  
 PIN1 : Gate 1 PIN2 : Gate 2

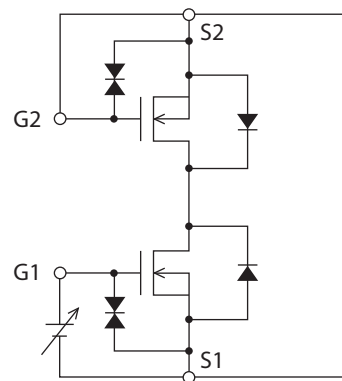
## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV <sub>SSS</sub>	Source-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>S</sub> =250uA	30			V
I <sub>SSS</sub>	Zero Gate Voltage Source Current	V <sub>SS</sub> =30V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±16V , V <sub>SS</sub> =0V			±10	uA
ON CHARACTERISTICS						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>SS</sub> =V <sub>GS</sub> , I <sub>S</sub> =1mA	1.0	1.5	2.5	V
R <sub>SS(ON)</sub>	Source-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>S</sub> =4.5A		7	8	m ohm
		V <sub>GS</sub> =4.5V , I <sub>S</sub> =4.5A		10	13	m ohm
DYNAMIC CHARACTERISTICS <sup>c</sup>						
C <sub>ISS</sub>	Input Capacitance	V <sub>SS</sub> =10V,V <sub>GS</sub> =0V f=1.0MHz		2870		pF
C <sub>OSS</sub>	Output Capacitance			410		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			154		pF
SWITCHING CHARACTERISTICS <sup>c</sup>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =15V I <sub>S</sub> =4.5A V <sub>GS</sub> =10V		42		ns
t <sub>r</sub>	Rise Time			168		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			538		ns
t <sub>f</sub>	Fall Time			396		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =15V,I <sub>S</sub> =9A, V <sub>GS</sub> =4.5V		22.8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V <sub>FSS</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V,I <sub>S</sub> =4.5A		0.8	1.2	V
Note						
a.Mounted on FR4 board of 25.4mm x 25.4mm x 1.0mm.						
b.Pulse Test:Pulse Width < 10us, Duty Cycle < 1%.						
c.Guaranteed by design, not subject to production testing.						

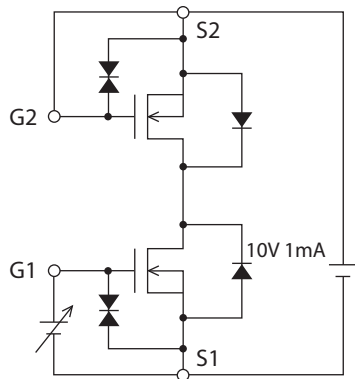
$V_{SSS} / I_{SSS}$



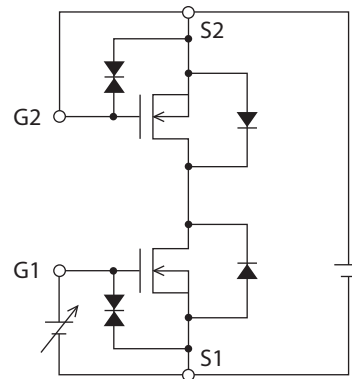
$I_{GSS} (+) / (-)$



$V_{GS} \text{ (off)}$

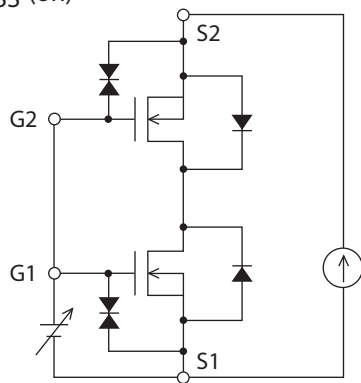


$|y_{fs}|$

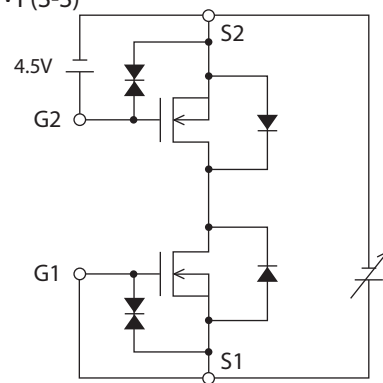


\* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

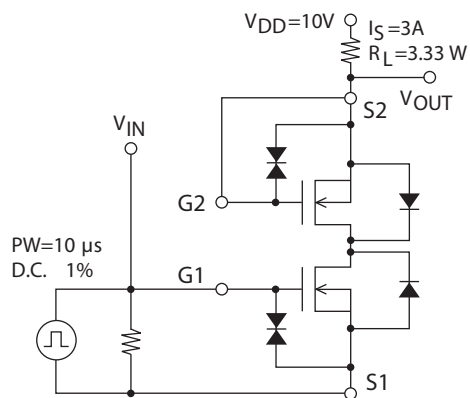
$R_{SS} \text{ (on)}$



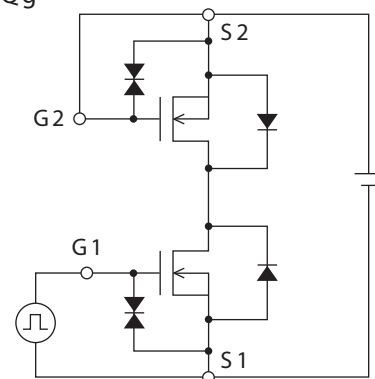
$V_F(S-S)$



$t_d(\text{on}), t_r, t_d(\text{off}), t_f$



$Q_g$



\* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

## TOP MARKING DEFINITION

### WLCSP

