



## Dual N-Channel Enhancement Mode Field Effect Transistor

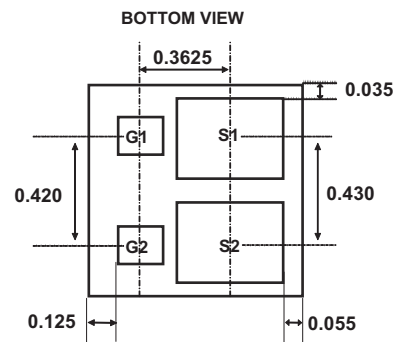
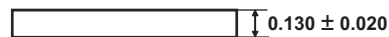
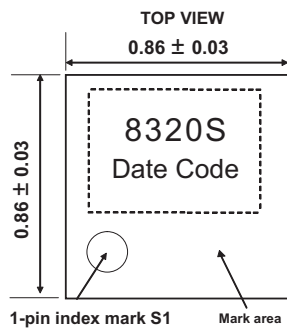
### PRODUCT SUMMARY

V <sub>SSS</sub>	I <sub>S</sub>	R <sub>SS(ON)</sub> (mΩ) Typ
20V	4.0A	45.0 @ V <sub>GS</sub> =4.5V
		48.0 @ V <sub>GS</sub> =4.0V
		57.0 @ V <sub>GS</sub> =3.1V
		70.0 @ V <sub>GS</sub> =2.5V

### FEATURES

- Super high dense cell design for low R<sub>SS(ON)</sub>.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.

### WLCSP



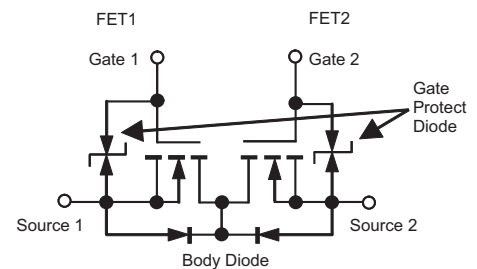
Gate oprn: 0.170x0.170 ; Source open: 0.425x0.340

S1: Source 1  
G1: Gate 1  
G2: Gate 2  
S2: Source 2

Unit : mm

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C)

Symbol	Parameter	Limit	Units
V <sub>SSS</sub>	Source-Source Voltage	20	V
V <sub>GSS</sub>	Gate-Source Voltage	±12	V
I <sub>S</sub>	Source Current-Continuous <sup>a</sup>	4	A
I <sub>SP</sub>	-Pulsed <sup>b</sup>	22	A
P <sub>T</sub>	Total Power Dissipation <sup>a</sup>	1.3	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C



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## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

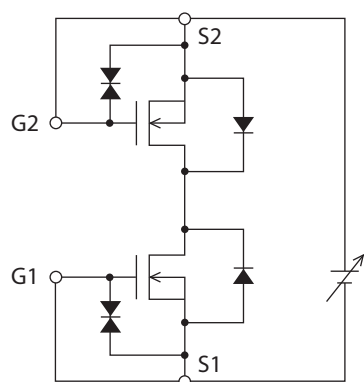
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV <sub>SSS</sub>	Source-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>S</sub> =250uA	20			V
I <sub>SSS</sub>	Zero Gate Voltage Source Current	V <sub>SS</sub> =12V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±8V , V <sub>SS</sub> =0V			±1	uA
ON CHARACTERISTICS						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>SS</sub> =V <sub>GS</sub> , I <sub>S</sub> =1mA	0.5	0.7	1.5	V
R <sub>SS(ON)</sub>	Source-Source On-State Resistance	V <sub>GS</sub> =4.5V , I <sub>S</sub> =2A	39	45	51	m ohm
		V <sub>GS</sub> =4.0V , I <sub>S</sub> =2A	40	48	55	m ohm
		V <sub>GS</sub> =3.1V , I <sub>S</sub> =2A	49	57	65	m ohm
		V <sub>GS</sub> =2.5V , I <sub>S</sub> =2A	60	70	80	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>SS</sub> =5V , I <sub>S</sub> =2A		11		S
DYNAMIC CHARACTERISTICS <sup>c</sup>						
C <sub>ISS</sub>	Input Capacitance	V <sub>SS</sub> =10V,V <sub>GS</sub> =0V f=1.0MHz		254		pF
C <sub>OSS</sub>	Output Capacitance			126		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			47		pF
SWITCHING CHARACTERISTICS <sup>c</sup>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =6V I <sub>S</sub> =1.5A V <sub>GS</sub> =4.5V R <sub>GEN</sub> =6 ohm		8		ns
t <sub>r</sub>	Rise Time			13		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			165		ns
t <sub>f</sub>	Fall Time			76		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =6V,I <sub>S</sub> =3A, V <sub>G1S1</sub> =4.5V		4.4		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V <sub>FSS</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V,I <sub>S</sub> =4A		0.76	1.2	V
Note						
a.Mounted on FR4 board of 25.4mm x 25.4mm x 1.6mm.						
b.Pulse Test:Pulse Width ≤ 10us, Duty Cycle ≤ 1%.						
c.Guaranteed by design, not subject to production testing.						

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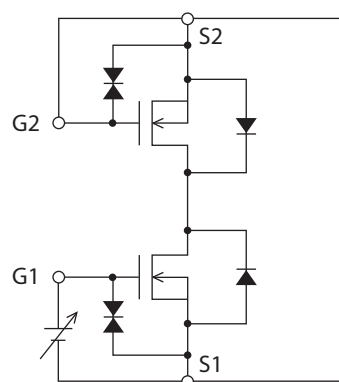
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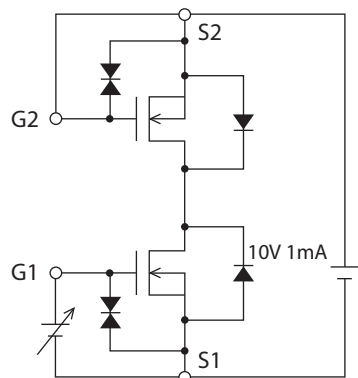
$V_{SSS} / I_{SSS}$



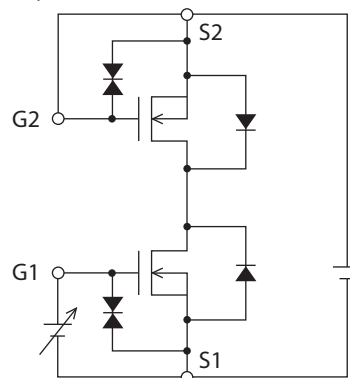
$I_{GSS} (+) / (-)$



$V_{GS} (off)$



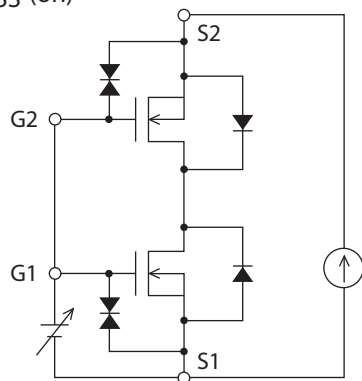
$|y_{fs}|$



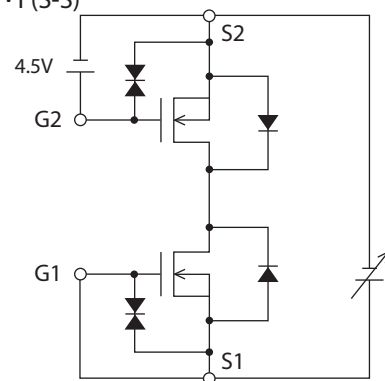
\* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

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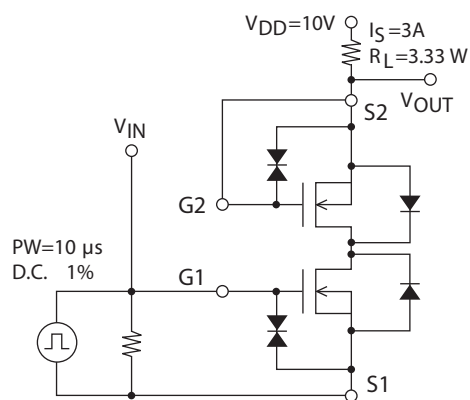
$R_{SS} \text{ (on)}$



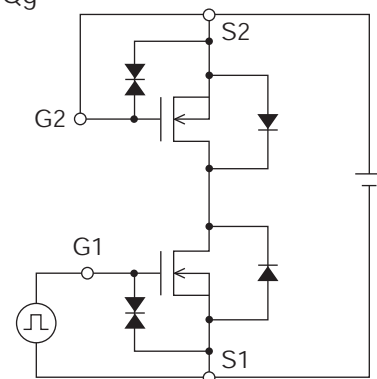
$V_{F(S-S)}$



$t_d(\text{on}), t_r, t_d(\text{off}), t_f$



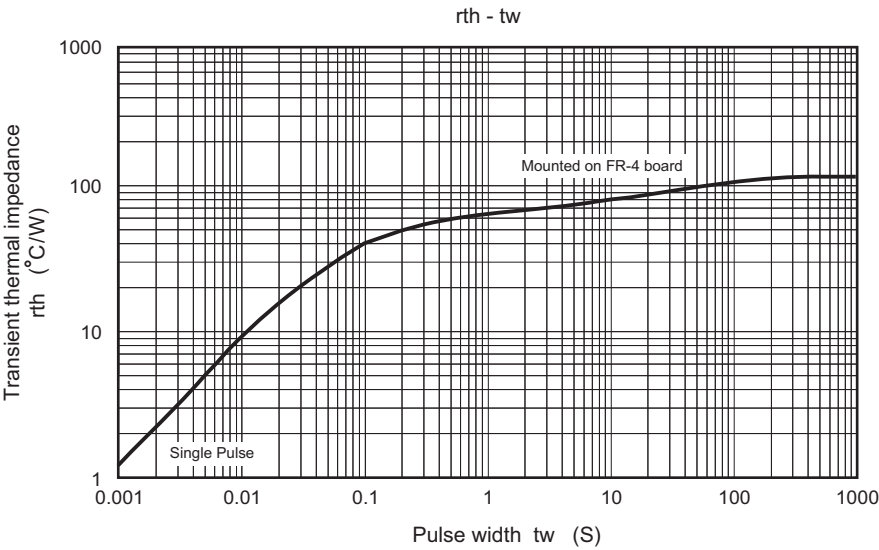
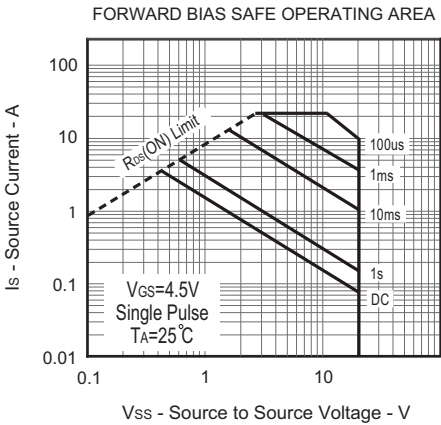
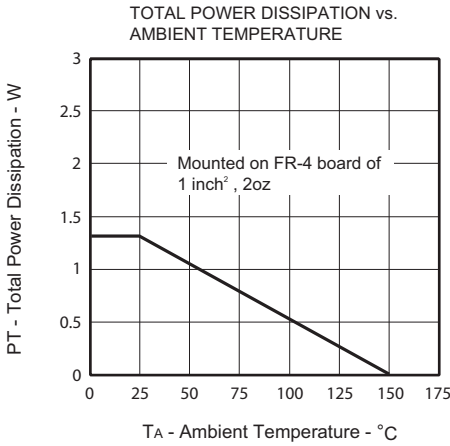
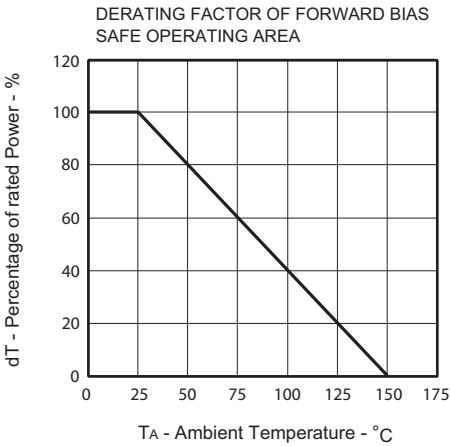
$Q_g$



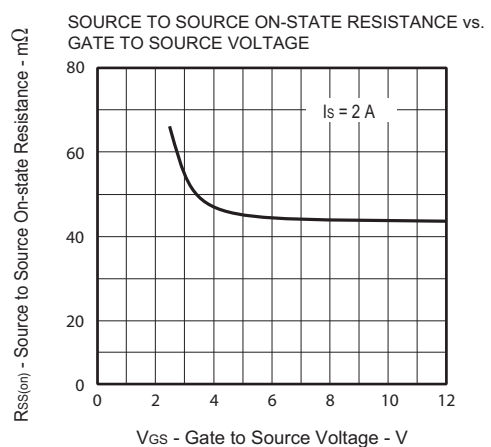
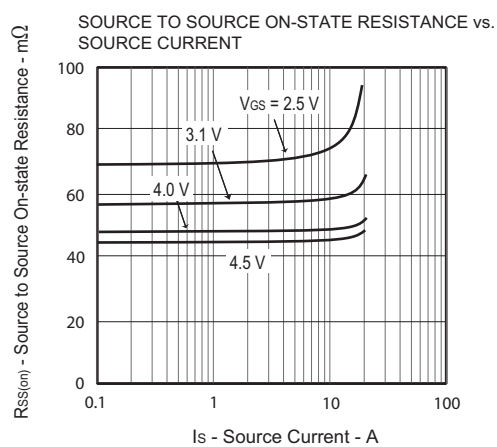
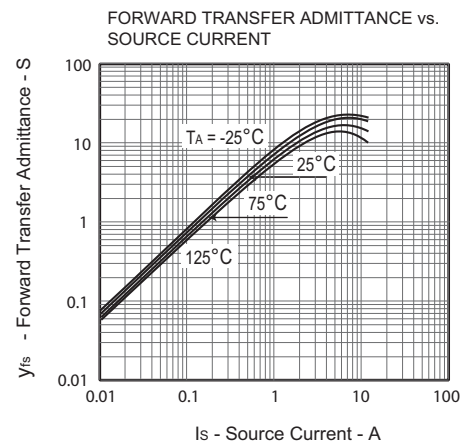
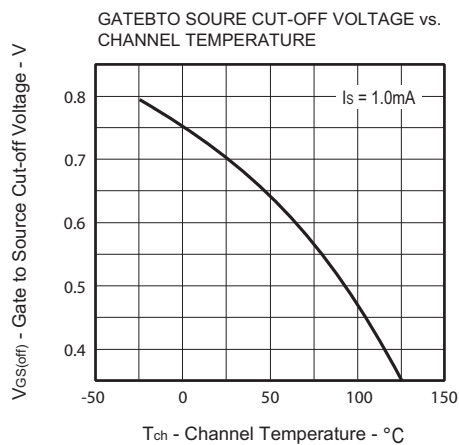
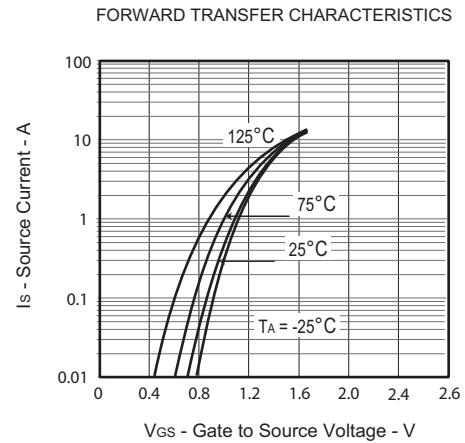
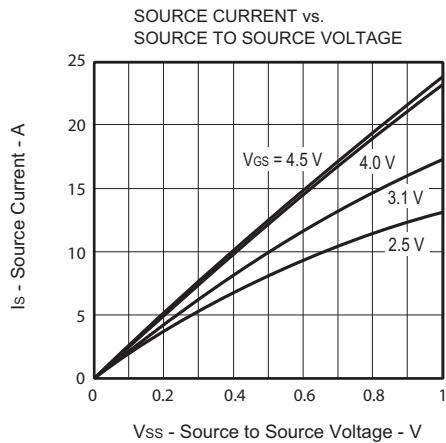
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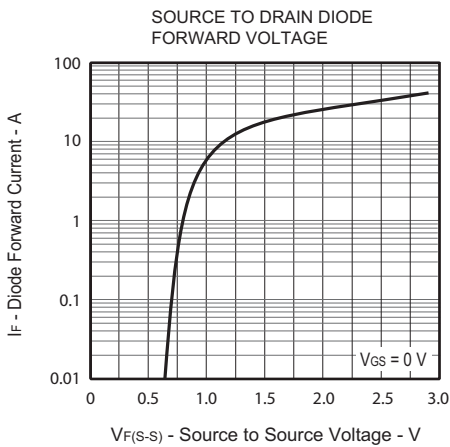
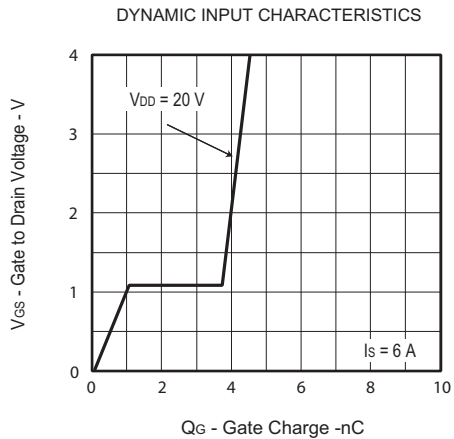
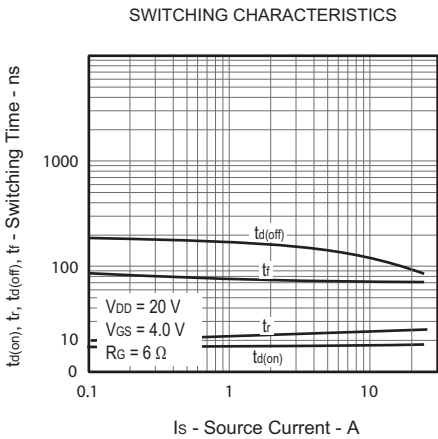
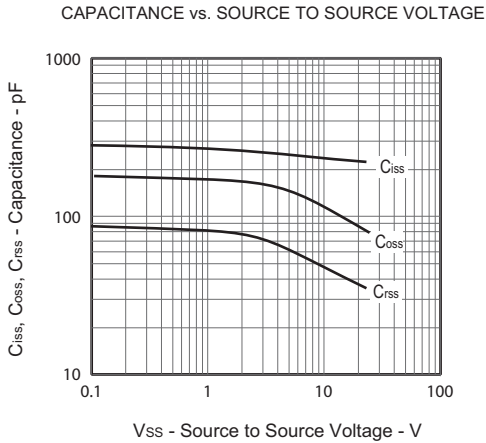
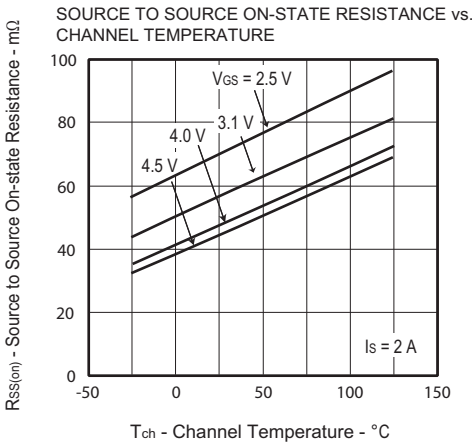
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## TOP MARKING DEFINITION

### WLCSP



Product No.

Wafer Lot No.

Production Month (1,2 ~ 9, A,B,C)

Production Year (2009 = 9, 2010 = A.....)

