



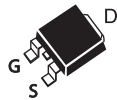
## P-Channel Logic Level Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

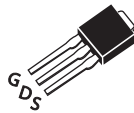
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
-40V	-27A	35 @ V <sub>GS</sub> =10V
		61 @ V <sub>GS</sub> =4.5V

### FEATURES

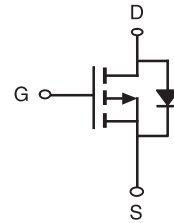
- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.



STU SERIES  
TO-252AA(D-PAK)



STD SERIES  
TO-251(I-PAK)



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	-40	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>C</sub> =25°C	-27
		T <sub>C</sub> =70°C	-21.6
I <sub>DM</sub>	-Pulsed <sup>b</sup>	-82	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	49	mJ
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> =25°C	42
		T <sub>C</sub> =70°C	27
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case <sup>a</sup>	3	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	50	°C/W

**ELECTRICAL CHARACTERISTICS** ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-32V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA
ON CHARACTERISTICS						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-1	-1.9	-3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =-10V , I <sub>D</sub> =-13.5A		28	35	m ohm
		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-10A		45	61	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-10V , I <sub>D</sub> =-13.5A		23		S
DYNAMIC CHARACTERISTICS <sup>°</sup>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-20V,V <sub>GS</sub> =0V f=1.0MHz		1025		pF
C <sub>oss</sub>	Output Capacitance			127		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			110		pF
SWITCHING CHARACTERISTICS <sup>°</sup>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-20V I <sub>D</sub> =-1.0A V <sub>GS</sub> =-10V R <sub>GEN</sub> = 6 ohm		18		ns
t <sub>r</sub>	Rise Time			19		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			68		ns
t <sub>f</sub>	Fall Time			25		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-20V,I <sub>D</sub> =-13.5A,V <sub>GS</sub> =-10V		22.5		nC
		V <sub>DS</sub> =-20V,I <sub>D</sub> =-13.5A,V <sub>GS</sub> =-4.5V		10.5		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-20V,I <sub>D</sub> =-13.5A, V <sub>GS</sub> =-10V		2.1		nC
Q <sub>gd</sub>	Gate-Drain Charge			6.5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I <sub>s</sub>	Maximum Continuous Drain-Source Forward Current				-2	A
V <sub>SD</sub>	Diode Forward Voltage <sup>b</sup>	V <sub>GS</sub> =0V,I <sub>s</sub> = -2A		-0.8	-1.3	V

**Notes**

- a.Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .  
b.Pulse Test:Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .  
c.Guaranteed by design, not subject to production testing.  
d.Starting  $T_J=25^{\circ}\text{C}$ ,  $L=0.5\text{mH}$ ,  $V_{DD}=20V$  .(See Figure13)

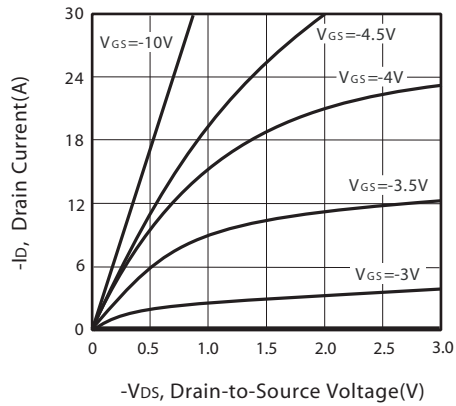


Figure 1. Output Characteristics

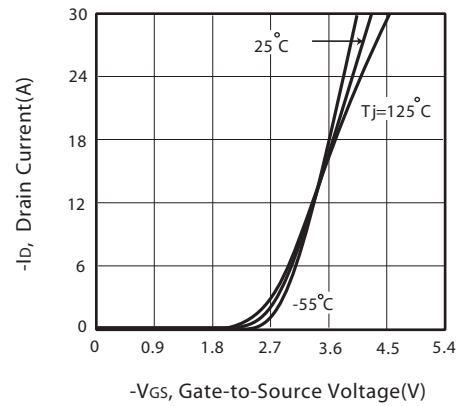


Figure 2. Transfer Characteristics

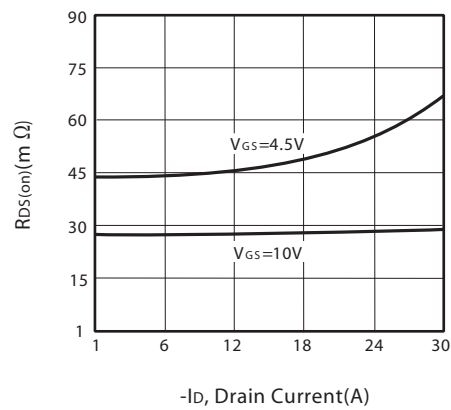


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

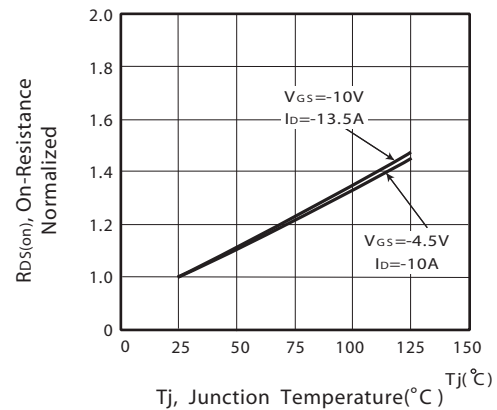


Figure 4. On-Resistance Variation with Drain Current and Temperature

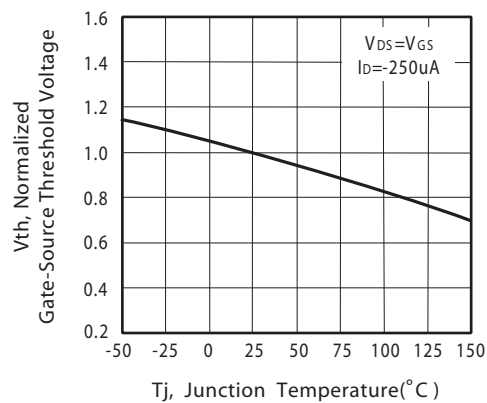


Figure 5. Gate Threshold Variation with Temperature

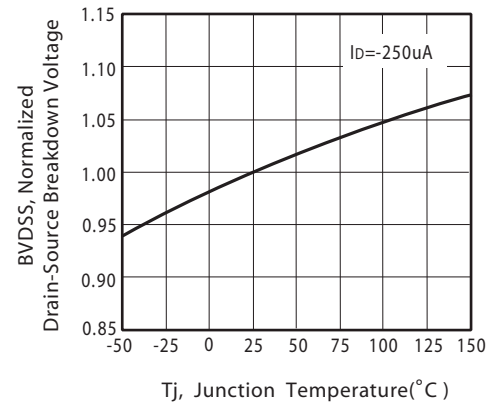


Figure 6. Breakdown Voltage Variation with Temperature

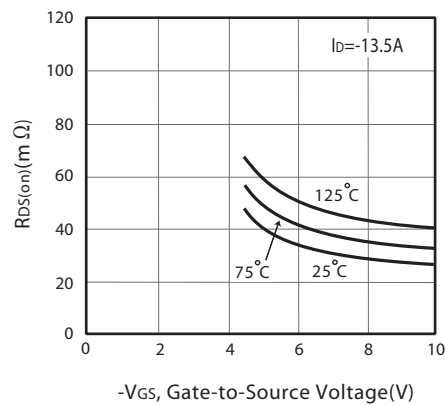


Figure 7. On-Resistance vs. Gate-Source Voltage

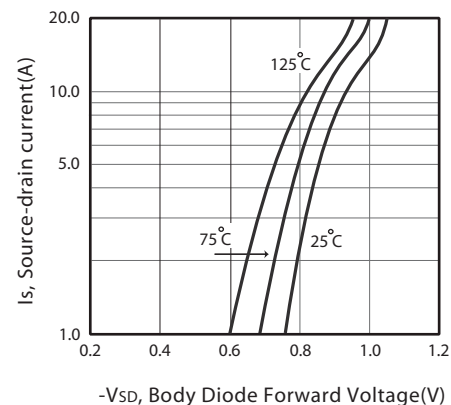


Figure 8. Body Diode Forward Voltage Variation with Source Current

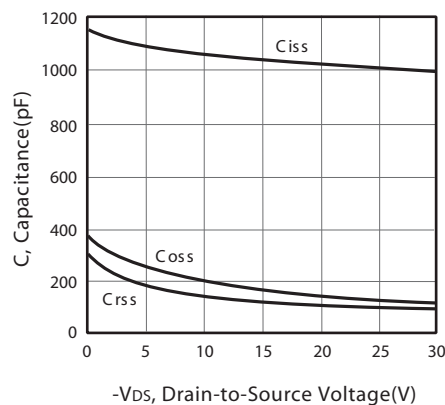


Figure 9. Capacitance

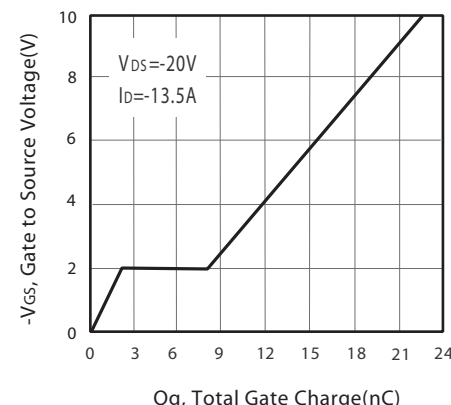


Figure 10. Gate Charge

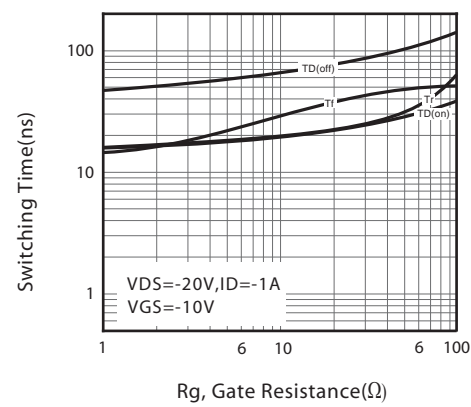


Figure 11. switching characteristics

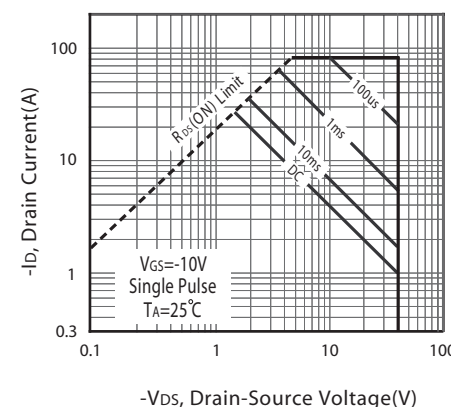
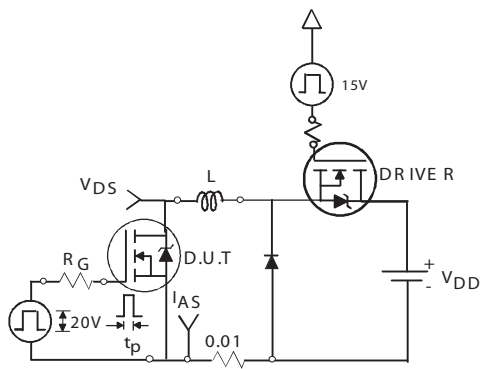
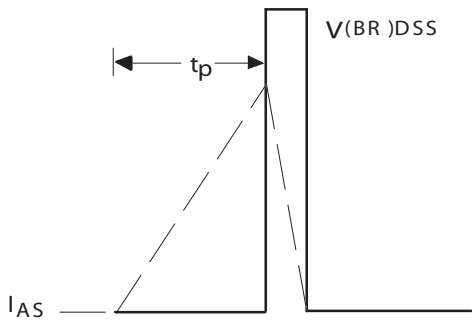


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

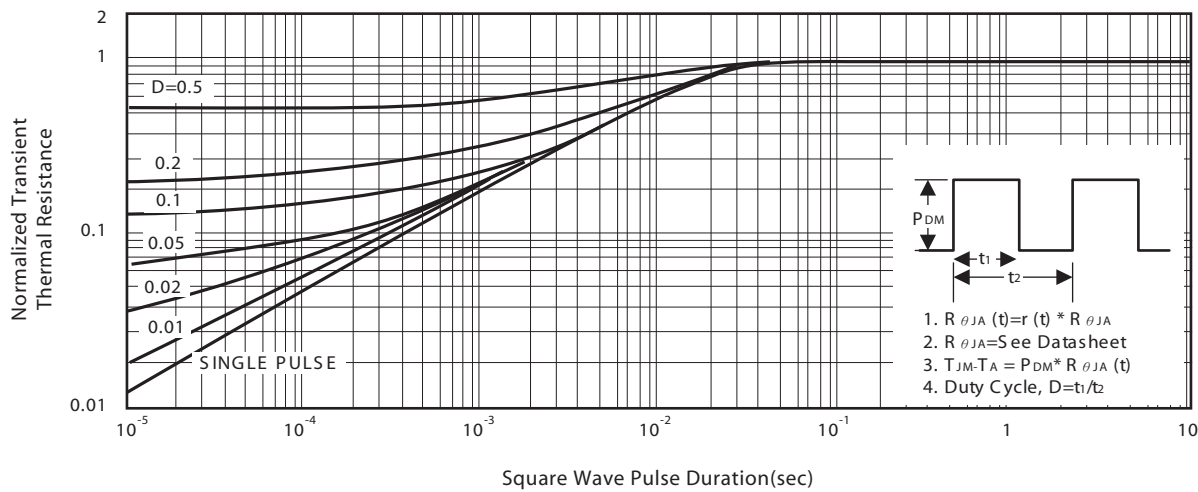
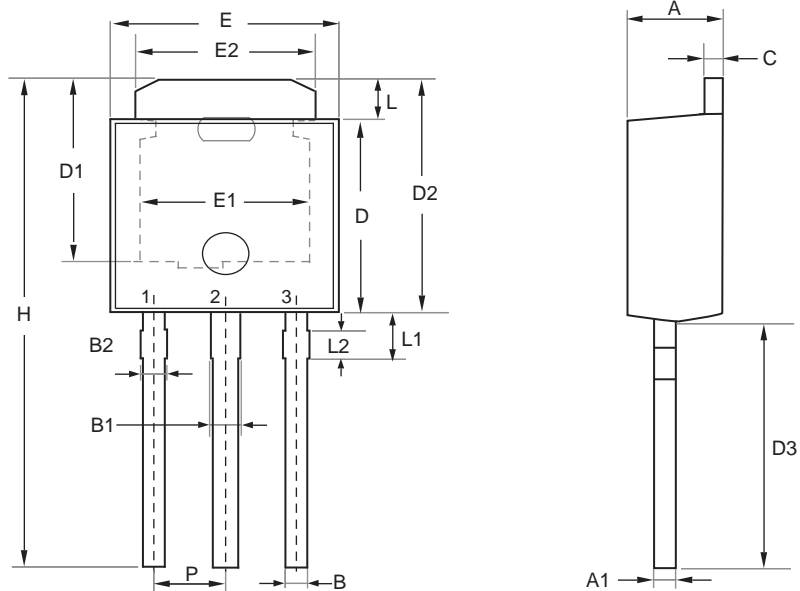


Figure 14. Normalized Thermal Transient Impedance Curve

## PACKAGE OUTLINE DIMENSIONS

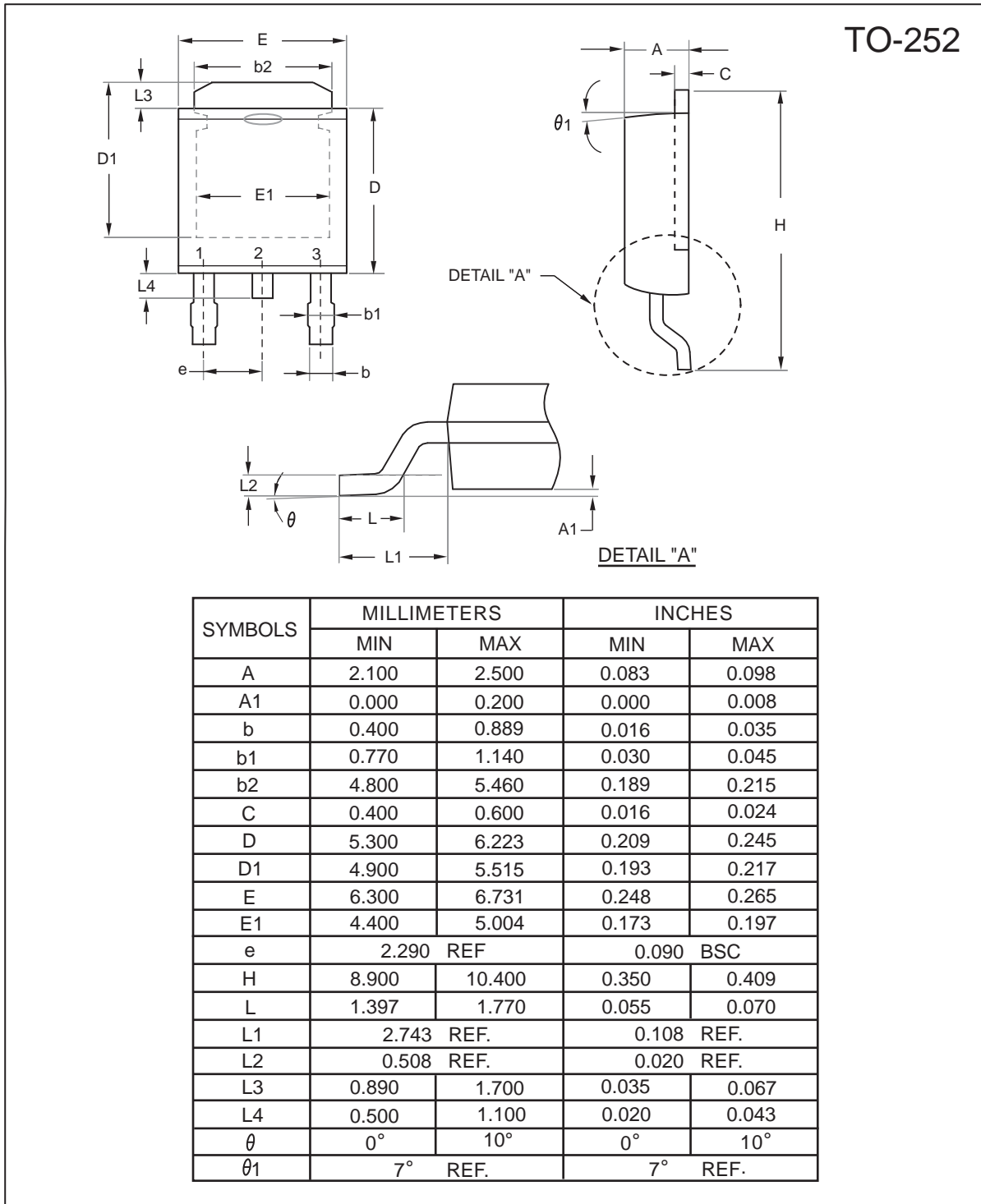
TO-251



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.100	2.500	0.083	0.098
A1	0.350	0.650	0.014	0.026
B	0.400	0.800	0.016	0.031
B1	0.650	1.050	0.026	0.041
B2	0.500	0.900	0.020	0.035
C	0.400	0.600	0.016	0.024
D	5.300	5.700	0.209	0.224
D1	4.900	5.300	0.193	0.209
D2	6.700	7.300	0.264	0.287
D3	7.000	8.000	0.276	0.315
H	10.830	11.430	0.426	0.450
E	6.300	6.700	0.248	0.264
E1	4.600	4.900	0.181	0.193
E2	4.800	5.200	0.189	0.205
L	1.300	1.700	0.051	0.067
L1	1.400	1.800	0.055	0.071
L2	0.500	0.900	0.020	0.035
P	2.300 BSC		0.091 BSC	

# STU/D441S

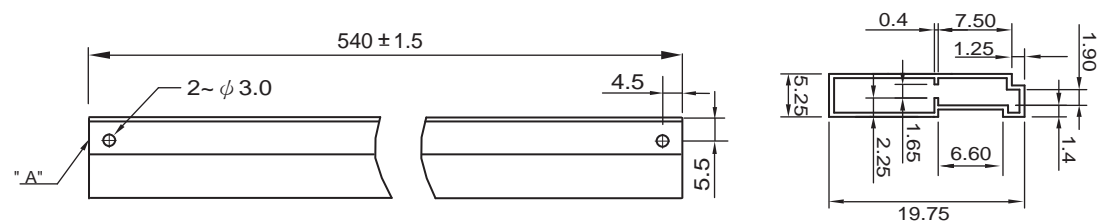
Ver 1.0



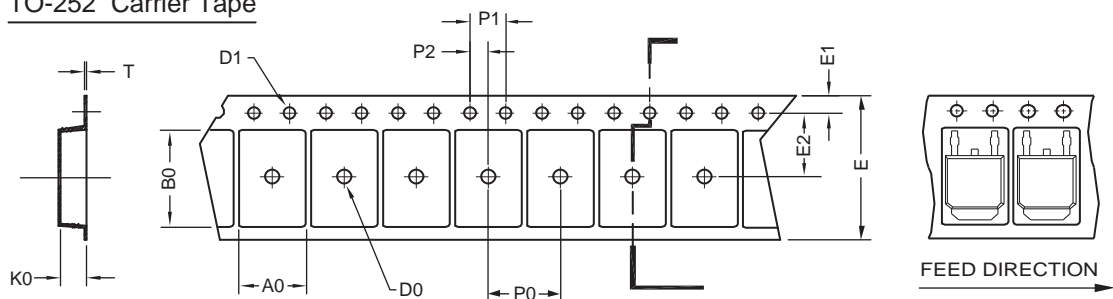
Feb,06,2010

TO251 Tube/TO-252 Tape and Reel Data

TO-251 Tube



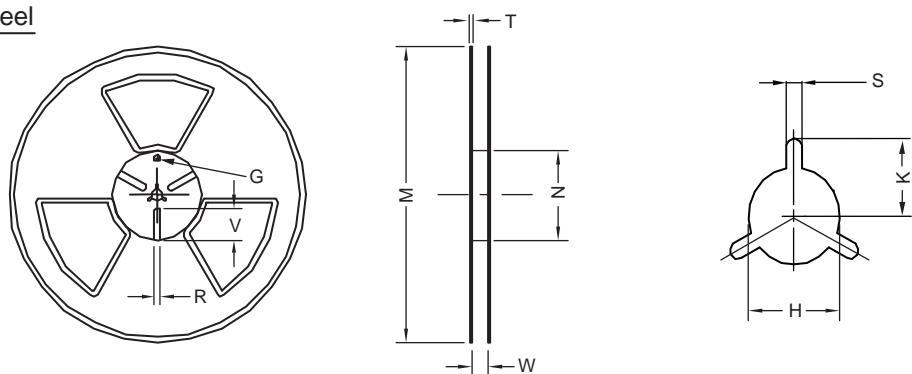
TO-252 Carrier Tape



UNIT:mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TO-252 (16 mm)	6.96 ±0.1	10.49 ±0.1	2.79 ±0.1	φ 2	φ 1.5 + 0.1 - 0	16.0 ±0.3	1.75 ±0.1	7.5 ±0.15	8.0 ±0.1	4.0 ±0.1	2.0 ±0.15	0.3 ±0.05

TO-252 Reel



UNIT:mm

TAPE SIZE	REEL SIZE	M	N	W	T	H	K	S	G	R	V
16 mm	φ 330	φ 330 ± 0.5	φ 97 ± 1.0	17.0 + 1.5 - 0	2.2	φ 13.0 + 0.5 - 0.2	10.6	2.0 ±0.5	---	---	---