SamHop Microelectronics Corp.

SP4510DG

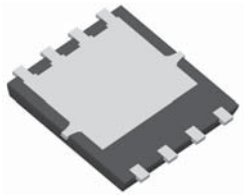
Ver 1.0

N-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V_{DSS}	I_D	$R_{DS(ON)}$ (mΩ) Max
100V	48A	19 @ VGS=10V

FEATURES

- Super high dense cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- Suface Mount Package.



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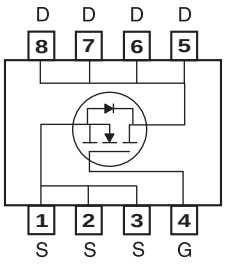


ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Symbol	Parameter		Limit	Units
V_{DS}	Drain-Source Voltage		100	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Drain Current-Continuous [c]	Tc=25°C	48	A
		Tc=70°C	38.4	A
I_{DM}	-Pulsed [a c]		98	A
E_{AS}	Single Pulse Avalanche Energy [d]		132	mJ
P_D	Maximum Power Dissipation	Tc=25°C	83	W
		Tc=70°C	53	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to 150	°C

THERMAL CHARACTERISTICS

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V , V_{GS}=0V			1	uA
I_{GSS}	Gate-Body leakage current	V_{GS}= ±20V , V_{DS}=0V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} , I_D=250uA	2.5	3.5	4.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V , I_D=24A		15	19	m ohm
g_{FS}	Forward Transconductance	V_{DS}=10V , I_D=24A		45		S
DYNAMIC CHARACTERISTICS [b]						
C_{ISS}	Input Capacitance	V_{DS}=25V,V_{GS}=0V f=1.0MHz		1460		pF
C_{OSS}	Output Capacitance			570		pF
C_{RSS}	Reverse Transfer Capacitance			65		pF
SWITCHING CHARACTERISTICS [b]						
$t_{D(ON)}$	Turn-On DelayTime	V_{DD}=50V I_D=1A V_{GS}=10V R_{GEN}= 2.5 ohm		10		ns
t_r	Rise Time			12		ns
$t_{D(OFF)}$	Turn-Off DelayTime			16		ns
t_f	Fall Time			7		ns
Q_g	Total Gate Charge	V_{DS}=50V,I_D=24A,V_{GS}=10V		25		nC
Q_{gs}	Gate-Source Charge	V_{DS}=50V,I_D=24A, V_{GS}=10V		8.4		nC
Q_{gd}	Gate-Drain Charge			7.8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_S=8A		0.82	1.3	V

Notes

a.Pulse Test:Pulse Width ≤ 10us, Duty Cycle ≤ 1%.
b.Guaranteed by design, not subject to production testing.
c.Drain current limited by maximum junction temperature.
d.Starting T_J=25°C,L=0.5mH,V_{DD} = 50V.(See Figure13)
e.Mounted on FR4 Board of 1 inch^2 , 2oz.

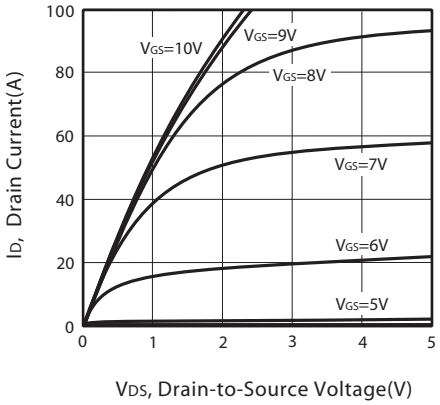


Figure 1. Output Characteristics

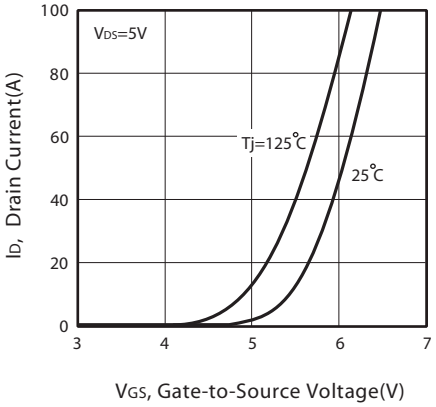


Figure 2. Transfer Characteristics

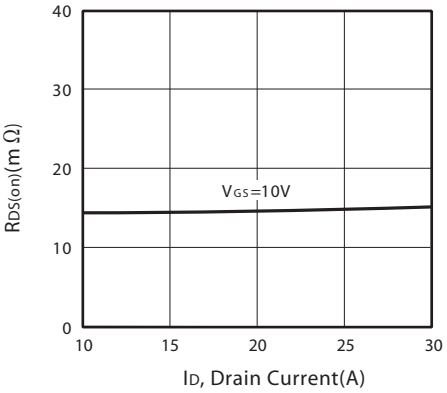


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

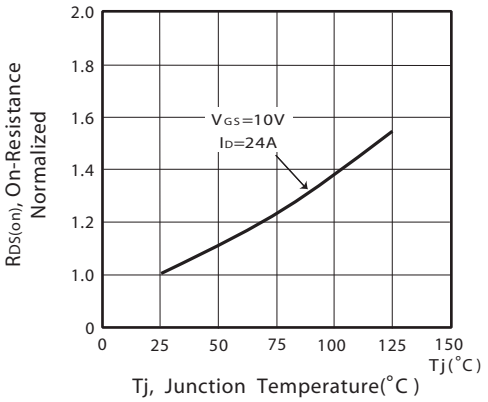


Figure 4. On-Resistance Variation with Drain Current and Temperature

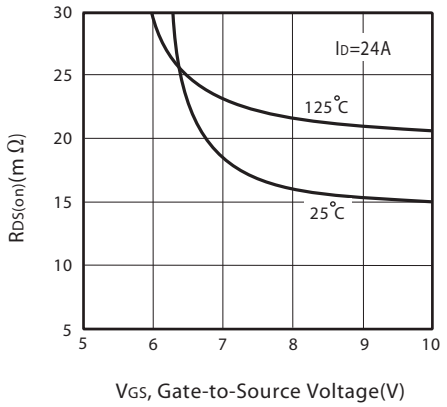


Figure 5. On-Resistance vs. Gate-Source Voltage

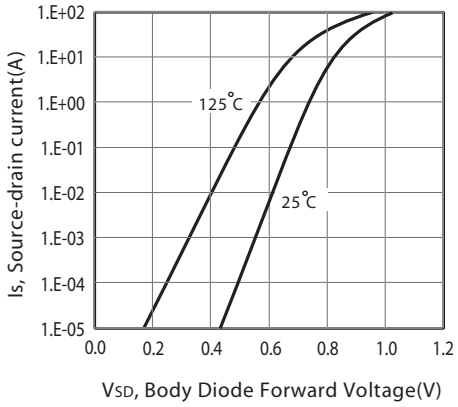


Figure 6. Body Diode Forward Voltage Variation with Source Current

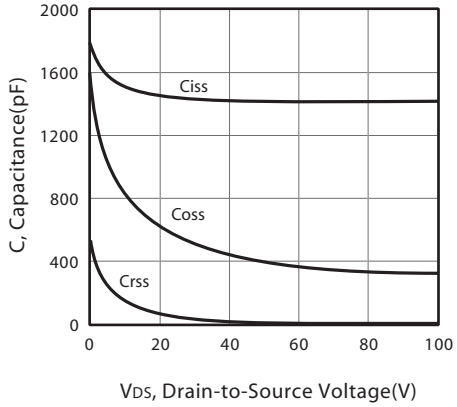


Figure 7. Capacitance

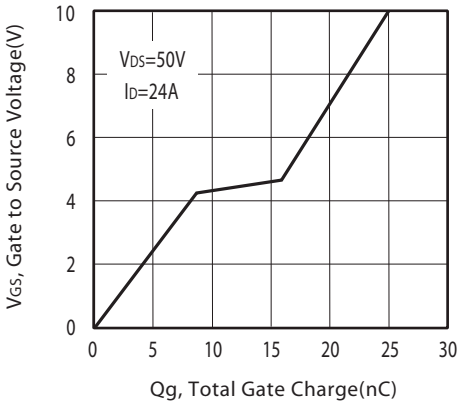


Figure 8. Gate Charge

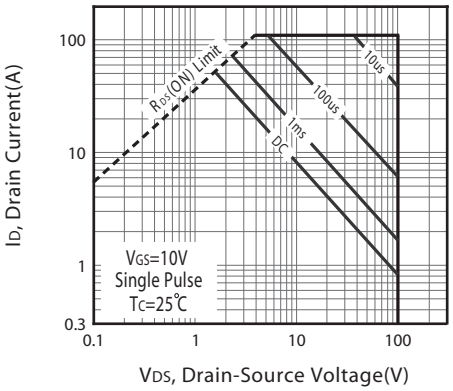
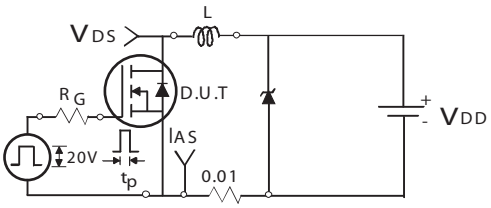
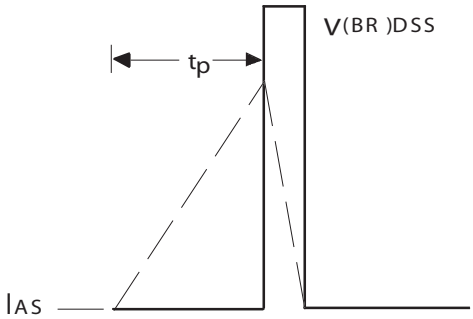


Figure 9. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

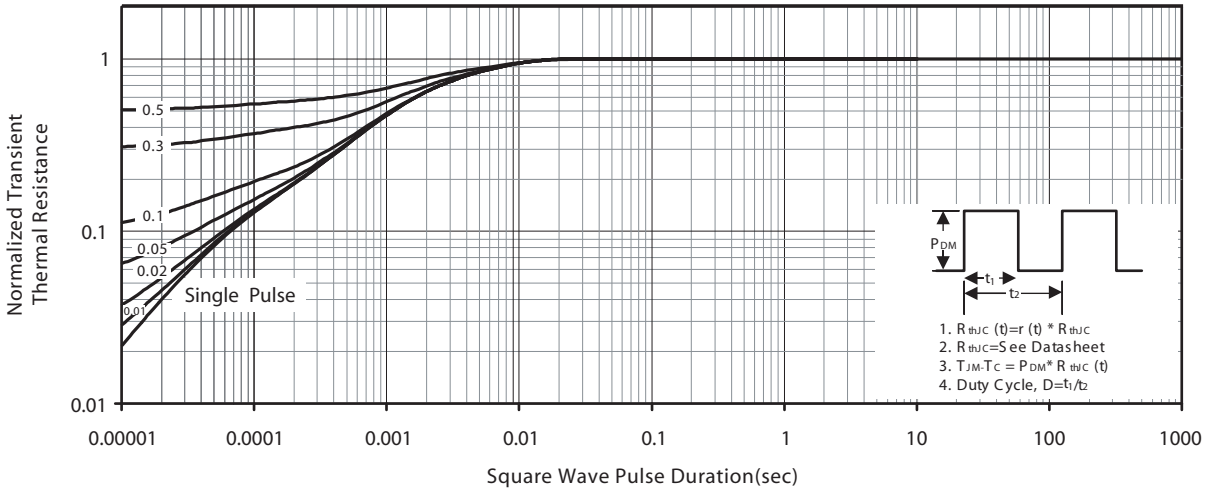


Figure 14. Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE DIMENSIONS

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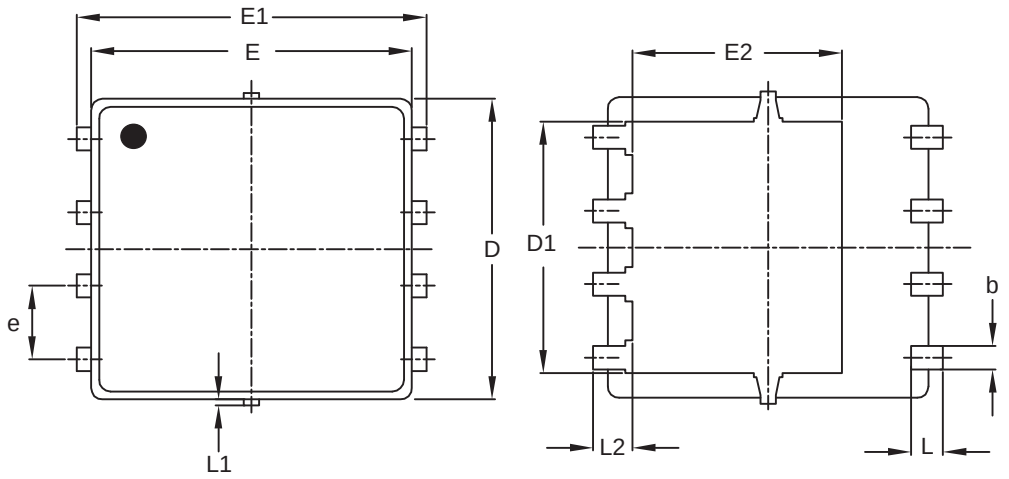
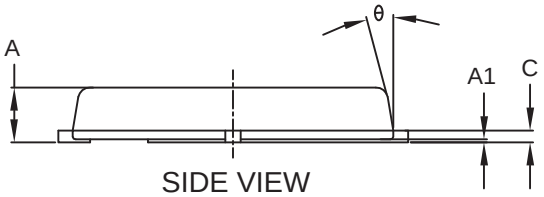


TOP VIEW

BOTTOM VIEW



SIDE VIEW

SYMBOLS	MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.95	1.00
A1	0.00	—	0.05
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D		5.20 BSC	
D1		4.35 BSC	
E		5.55 BSC	
E1		6.05 BSC	
E2		3.62 BSC	
e		1.27 BSC	
L	0.45	0.55	0.65
L1	0.00	—	0.15
L2		0.68 REF	
θ	0°	—	10°

TOP MARKING DEFINITION

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