



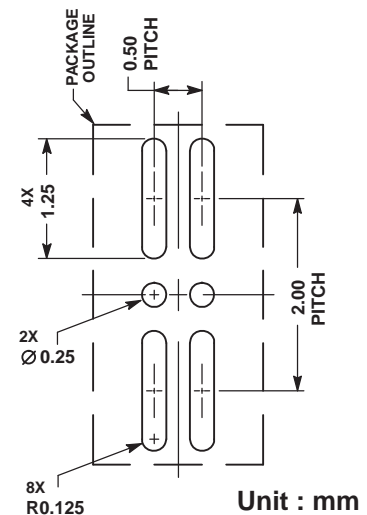
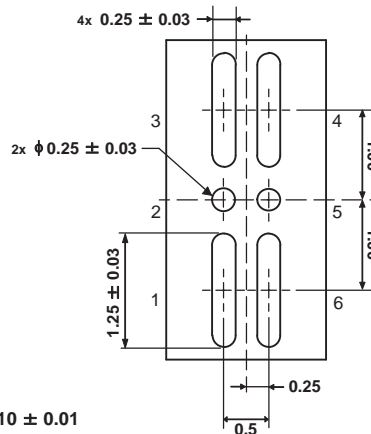
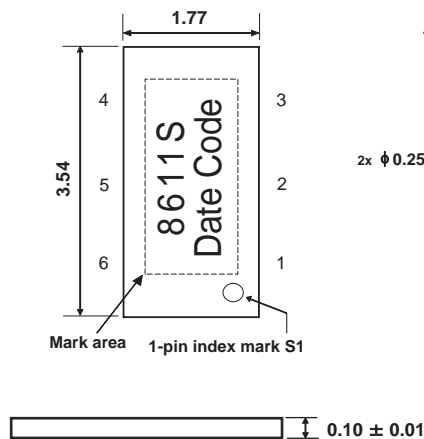
Ver 2.0

PRODUCT SUMMARY

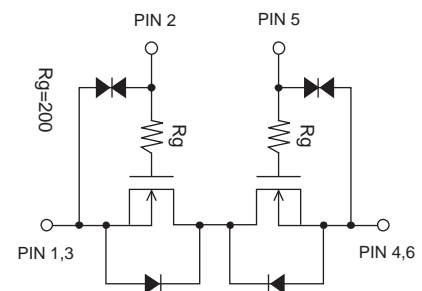
VSSS	IS	RSS(ON) (mΩ) Typ
12V	11A	2.4 @ VGS=4.5V
		2.5 @ VGS=4.0V
		2.6 @ VGS=3.8V
		3.3 @ VGS=3.1V
		4.0 @ VGS=2.5V

- Super high dense cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.

LAND PATTERN (REFERENCE)



Symbol	Parameter	Limit	Units
V _{SSS}	Source-Source Voltage	12	V
V _{GSS}	Gate-Source Voltage	±8	V
I _S	Source Current-Continuous ^c	11	A
I _{SP}	-Pulsed ^{a c}	110	A
P _T	Total Power Dissipation	2.5	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C



PIN 1 : Source 1
PIN 2 : Gate 1
PIN 3 : Source 1
PIN 4 : Source 2
PIN 5: Gate 2
PIN 6 : Source 2

SC8611S

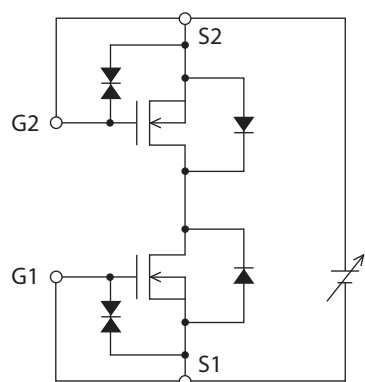
Ver 2.0

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

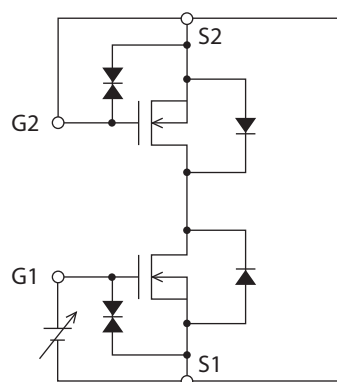
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{SSS}	Source-Source Breakdown Voltage	V _{GS} =0V, I _S =1mA	12			V
I _{SSS}	Zero Gate Voltage Source Current	V _{SS} =10V, V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±5V, V _{SS} =0V			±1	uA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{SS} =V _{GS} , I _S =1mA	0.5		1.3	V
R _{SS(ON)}	Source-Source On-State Resistance	V _{GS} =4.5V, I _S =5.5A	1.7	2.4	3.0	m ohm
		V _{GS} =4.0V, I _S =5.5A	1.9	2.5	3.3	m ohm
		V _{GS} =3.8V, I _S =5.5A	2.0	2.6	3.4	m ohm
		V _{GS} =3.1V, I _S =5.5A	2.3	3.3	4.6	m ohm
		V _{GS} =2.5V, I _S =5.5A	2.5	4.0	6.7	m ohm
g _{FS}	Forward Transconductance	V _{SS} =5V, I _S =5.5A		19		S
SWITCHING CHARACTERISTICS^b						
t _{D(ON)}	Turn-On Delay Time	V _{SS} =6V I _S =5.5A V _{GS} =4.5V		80		ns
t _r	Rise Time			570		ns
t _{D(OFF)}	Turn-Off Delay Time			38000		ns
t _f	Fall Time			17700		ns
Q _g	Total Gate Charge	V _{SS} =6V, I _S =5.5A, V _{GS} =4.5V		100		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V _{FSS}	Diode Forward Voltage	V _{GS} =0V, I _S =3A		0.75	1.2	V
Notes a. Pulse Test: Pulse Width ≤ 10us, Duty Cycle ≤ 1%. b. Guaranteed by design, not subject to production testing. c. Drain current limited by maximum junction temperature.						

Mar, 16, 2017

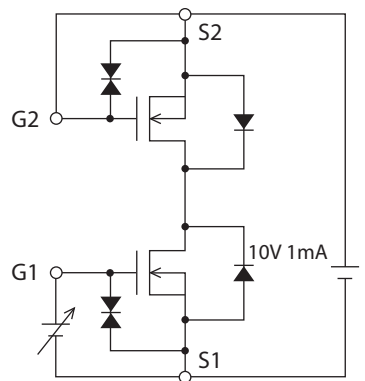
V_{SSS} / I_{SSS}



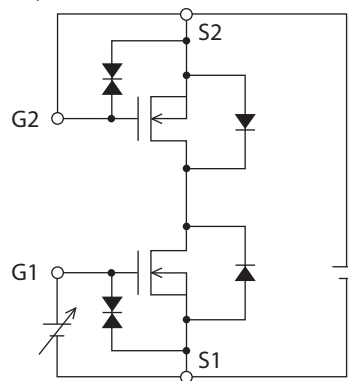
$I_{GSS} (+) / (-)$



$V_{GS} (off)$

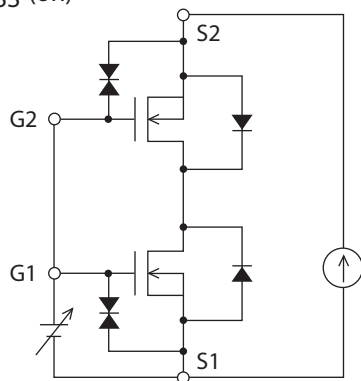


$|y_{fs}|$

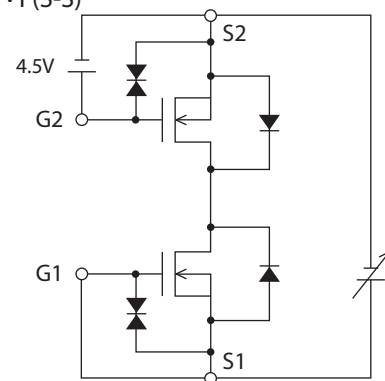


* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

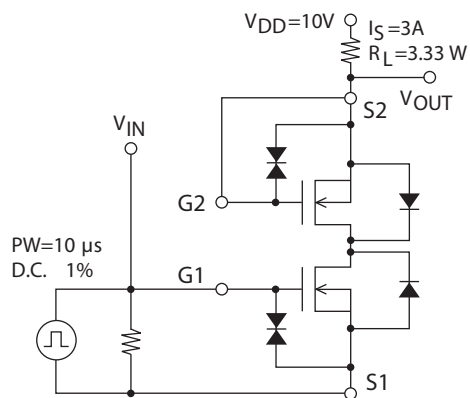
$R_{SS} \text{ (on)}$



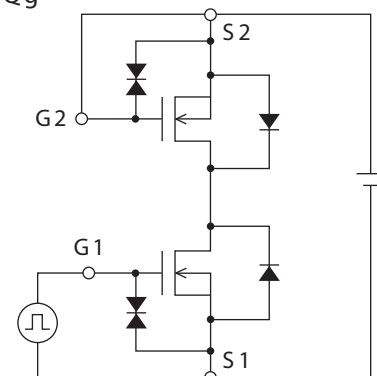
$V_F(S-S)$



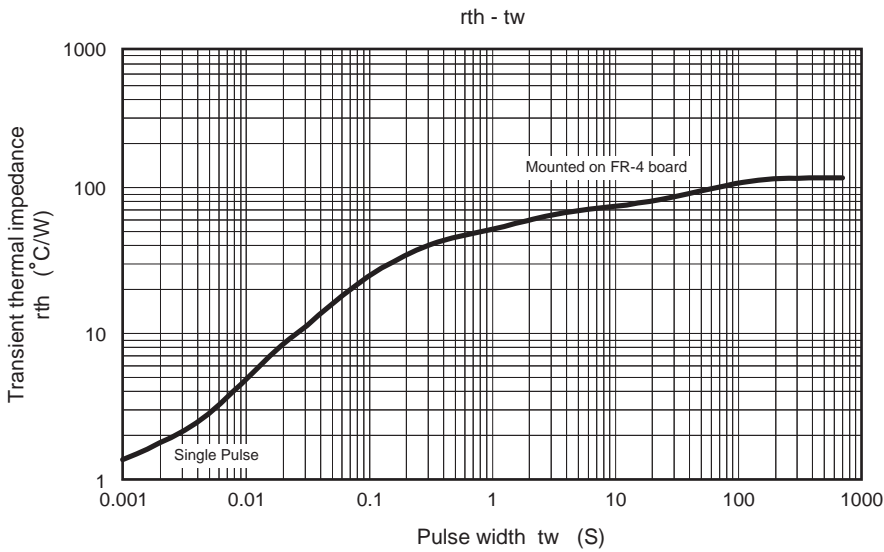
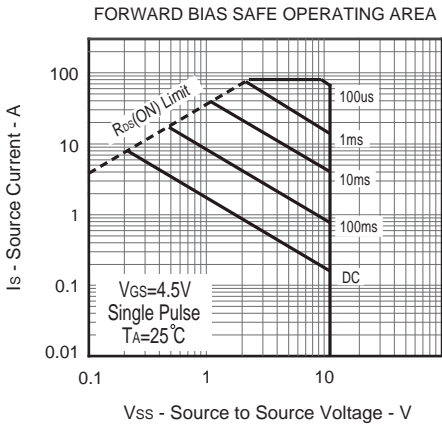
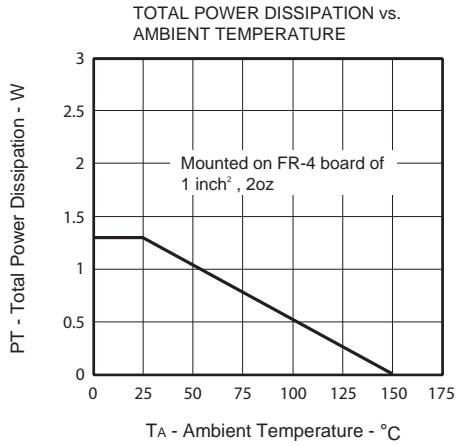
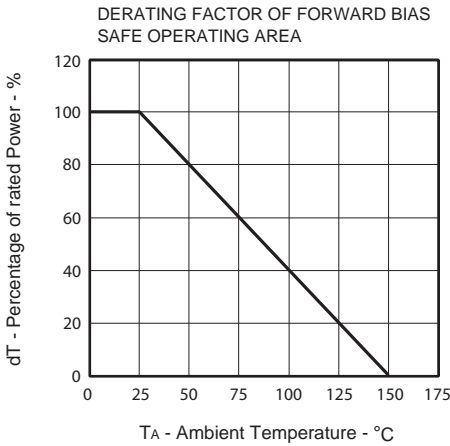
$t_d(\text{on}), t_r, t_d(\text{off}), t_f$

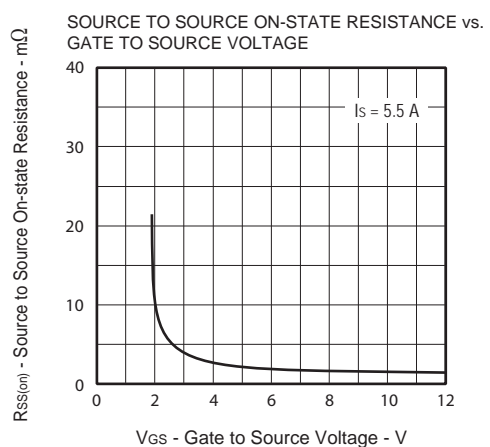
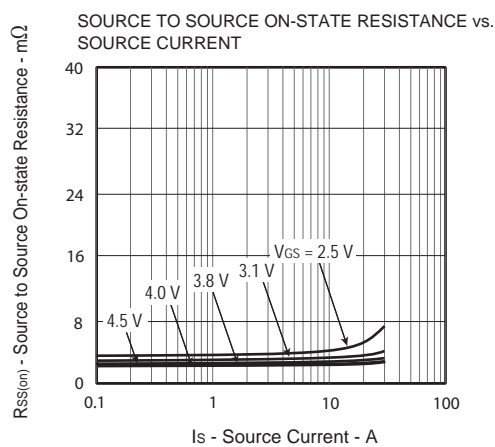
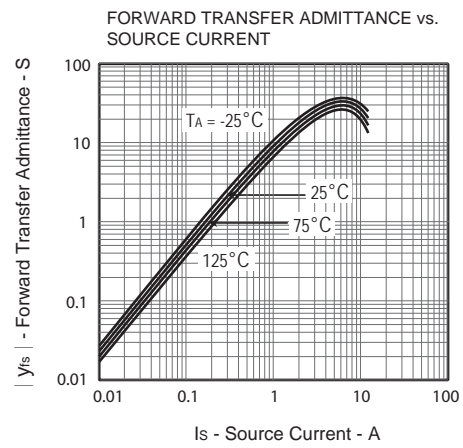
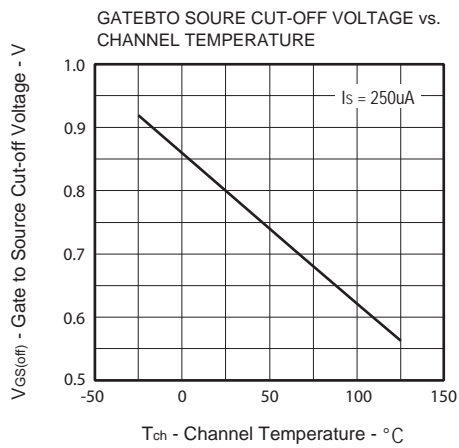
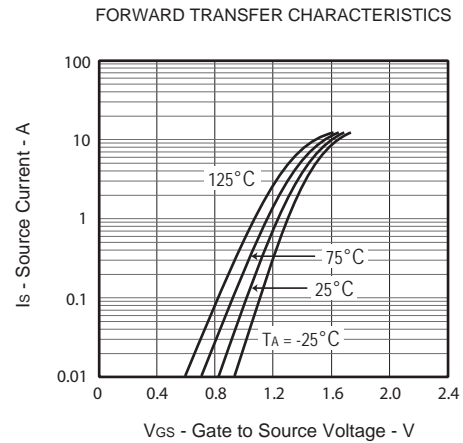
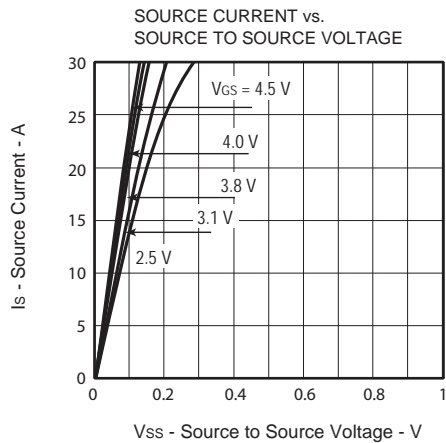


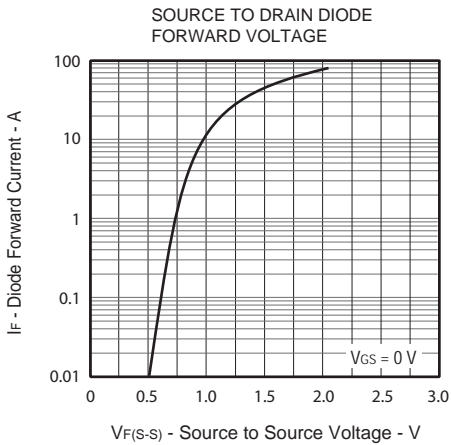
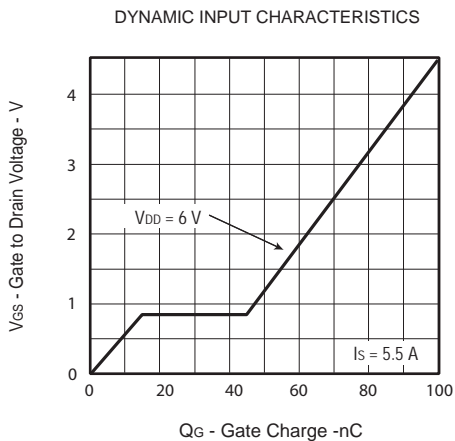
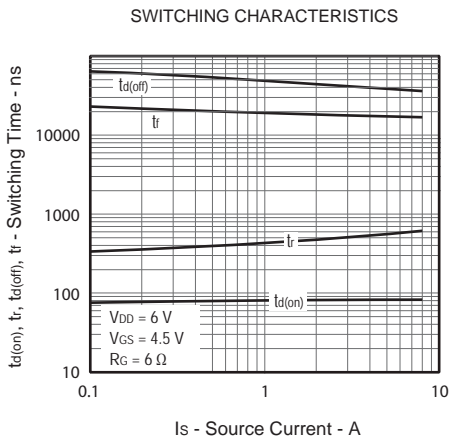
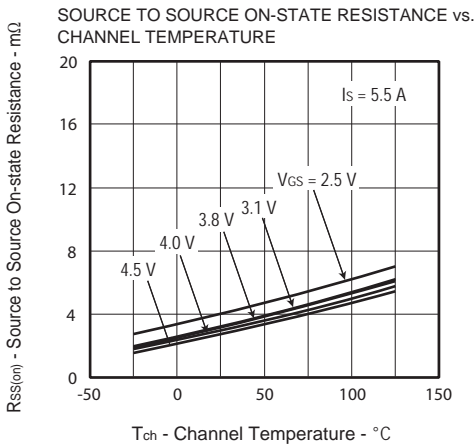
Q_g



* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.







TOP MARKING DEFINITION

