

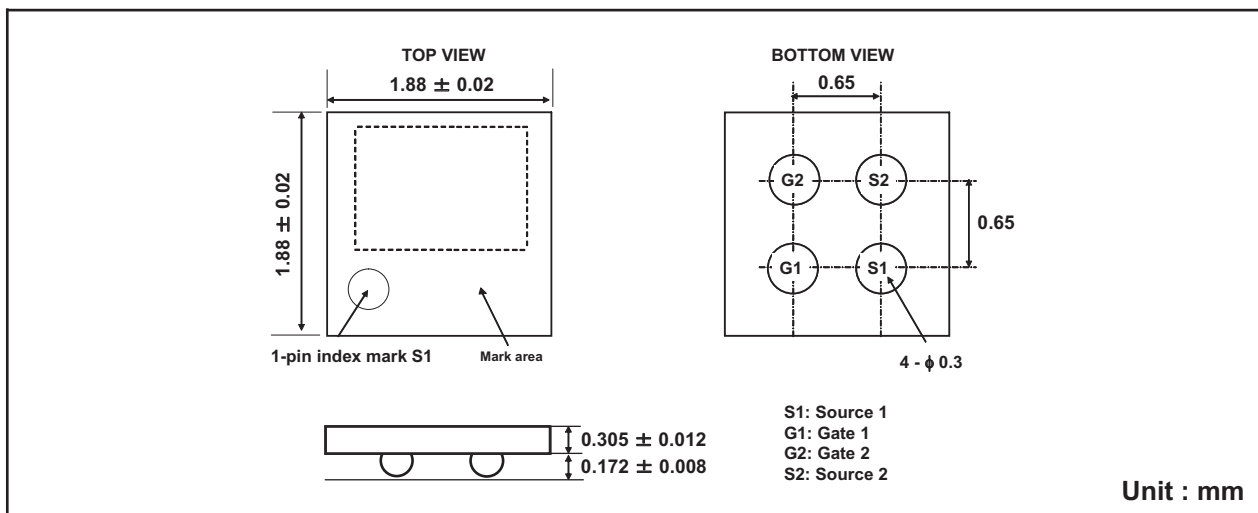


Dual N-Channel Enhancement Mode Field Effect Transistor

| PRODUCT SUMMARY | | |
|------------------|----------------|------------------------------|
| V _{SSS} | I _S | R _{SS(ON)} (mΩ) Max |
| 24V | 6A | 23.0 @ V _{GS} =4.5V |
| | | 24.0 @ V _{GS} =4.0V |
| | | 25.5 @ V _{GS} =3.1V |
| | | 35.0 @ V _{GS} =2.5V |

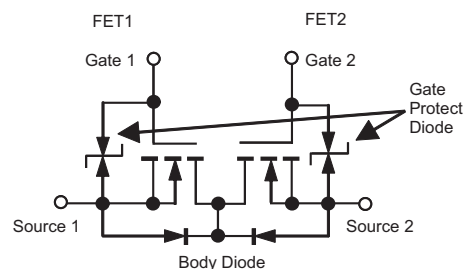
FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.



ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

| Symbol | Parameter | Limit | Units |
|-----------------------------------|--|------------|-------|
| V _{SSS} | Source-Source Voltage | 24 | V |
| V _{GSS} | Gate-Source Voltage | ±12 | V |
| I _S | Source Current-Continuous ^a | 6 | A |
| I _{SP} | -Pulsed ^b | 60 | A |
| P _T | Total Power Dissipation ^a | 1.6 | W |
| T _J , T _{STG} | Operating Junction and Storage Temperature Range | -55 to 150 | °C |



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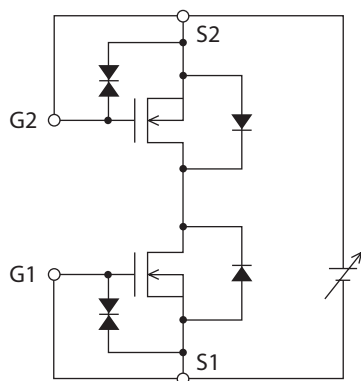
Ver 1.1

ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

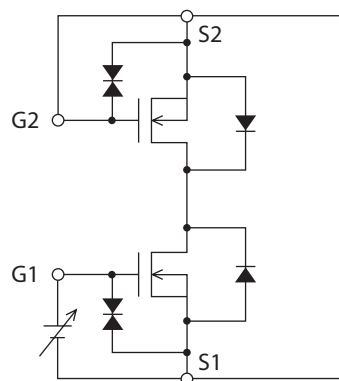
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|-----------------------------------|--|------|------|------|-------|
| OFF CHARACTERISTICS | | | | | | |
| BV _{SSS} | Source-Source Breakdown Voltage | V _{GS} =0V , I _S =250uA | 24 | | | V |
| I _{SSS} | Zero Gate Voltage Source Current | V _{SS} =24V , V _{GS} =0V | | | 1 | uA |
| I _{GSS} | Gate-Body Leakage Current | V _{GS} = ±12V , V _{SS} =0V | | | ±10 | uA |
| ON CHARACTERISTICS | | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | V _{SS} =V _{GS} , I _S =1mA | 0.5 | 0.86 | 1.5 | V |
| R _{SS(ON)} | Source-Source On-State Resistance | V _{GS} =4.5V , I _S =3A | 13.5 | 19.5 | 23.0 | m ohm |
| | | V _{GS} =4.0V , I _S =3A | 14.0 | 20.5 | 24.0 | m ohm |
| | | V _{GS} =3.1V , I _S =3A | 14.5 | 22.0 | 25.5 | m ohm |
| | | V _{GS} =2.5V , I _S =3A | 15.9 | 28.0 | 35.0 | m ohm |
| g _{FS} | Forward Transconductance | V _{SS} =5V , I _S =3A | | 14 | | S |
| DYNAMIC CHARACTERISTICS ^c | | | | | | |
| C _{ISS} | Input Capacitance | V _{SS} =10V, V _{GS} =0V f=1.0MHz | | 437 | | pF |
| C _{OSS} | Output Capacitance | | | 205 | | pF |
| C _{RSS} | Reverse Transfer Capacitance | | | 77 | | pF |
| SWITCHING CHARACTERISTICS ^c | | | | | | |
| t _{D(ON)} | Turn-On Delay Time | V _{DD} =20V I _S =3A | | 280 | | ns |
| t _r | Rise Time | | | 1120 | | ns |
| t _{D(OFF)} | Turn-Off Delay Time | V _{GS} =4.0V R _{GEN} =6 ohm | | 3580 | | ns |
| t _f | Fall Time | | | 2640 | | ns |
| Q _g | Total Gate Charge | V _{DD} =20V, I _S =6A, V _{G1S1} =4.0V | | 15.2 | | nC |
| DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS | | | | | | |
| V _{FSS} | Diode Forward Voltage | V _{GS} =0V, I _S =1.5A | | 0.77 | 1.2 | V |
| Note a. Mounted on FR4 board of 25.4mm x 25.4mm x 1.6mm. b. Pulse Test: Pulse Width ≤ 10us, Duty Cycle ≤ 1%. c. Guaranteed by design, not subject to production testing. | | | | | | |

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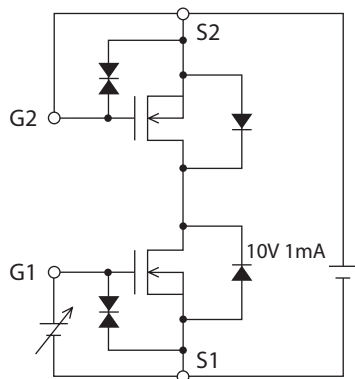
V_{SSS} / I_{SSS}



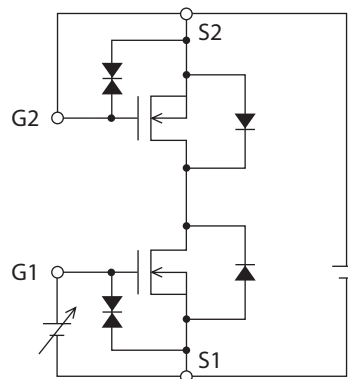
$I_{GSS} (+) / (-)$



$V_{GS} (off)$



$|y_{fs}|$

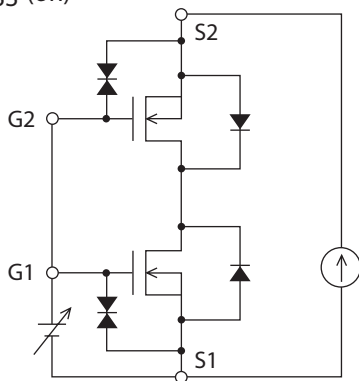


* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

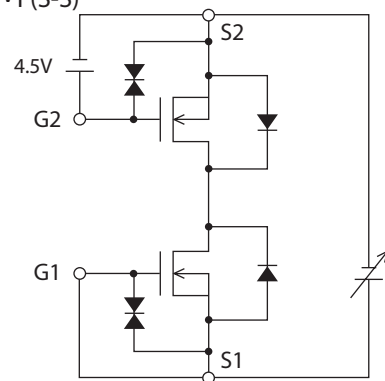
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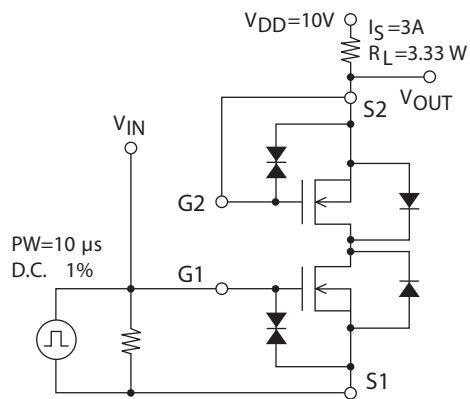
$R_{SS} \text{ (on)}$



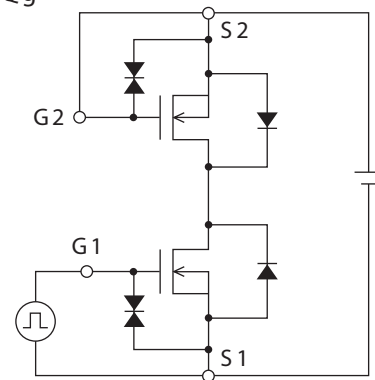
$V_F \text{ (S-S)}$



$t_d \text{ (on)}, t_r, t_d \text{ (off)}, t_f$



Q_g



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